

The closed-loop gain must be 3.0 for oscillations to be sustained. For an inverting amplifier, the gain is that of a noninverting amplifier.

$$A_v = \frac{R_f}{R_i} + 1$$

R_i is composed of R_3 (the source resistor) and r'_{ds} . Substituting,

$$A_v = \frac{R_f}{R_3 + r'_{ds}} + 1$$

Rearranging and solving for R_f ,

$$R_f = (A_v - 1)(R_3 + r'_{ds}) = (3 - 1)(1.0 \text{ k}\Omega + 500 \Omega) = 3.0 \text{ k}\Omega$$

Related Problem*

What happens to the oscillations if the setting of R_f is too high? What happens if the setting is too low?

*Answers are at the end of the chapter.



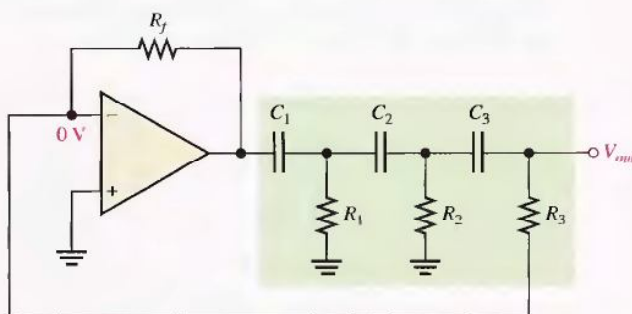
Open the Multisim file E16-01 in the Examples folder on your CD-ROM. Determine the frequency of oscillation and compare with the calculated value.

The Phase-Shift Oscillator

Figure 16-13 shows a sinusoidal feedback oscillator called the **phase-shift oscillator**. Each of the three RC circuits in the feedback loop can provide a *maximum* phase shift approaching 90° . Oscillation occurs at the frequency where the total phase shift through the three RC circuits is 180° . The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop.

FIGURE 16-13

Phase-shift oscillator.



The attenuation, B , of the three-section RC feedback circuit is

Equation 16-3

$$B = \frac{1}{29}$$

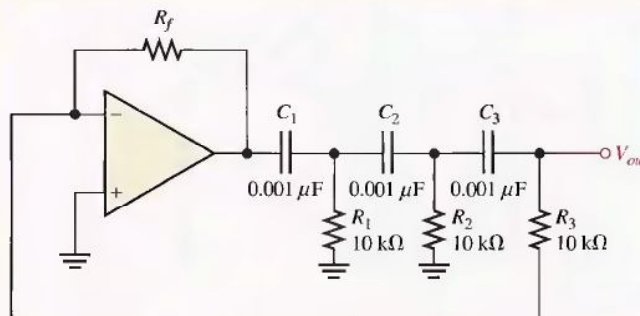
where $B = R_3/R_f$. The derivation of this unusual result is given in Appendix B. To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by R_f and R_3). The frequency of oscillation (f_r) is also derived in Appendix B and is stated in the following equation, where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

Equation 16-4

$$f_r = \frac{1}{2\pi\sqrt{6RC}}$$

EXAMPLE 16-2

- (a) Determine the value of R_f necessary for the circuit in Figure 16-14 to operate as an oscillator.
- (b) Determine the frequency of oscillation.

► **FIGURE 16-14**

Solution (a) $A_{cl} = 29$, and $B = 1/29 = R_3/R_f$. Therefore,

$$\frac{R_f}{R_3} = 29$$

$$R_f = 29R_3 = 29(10 \text{ k}\Omega) = 290 \text{ k}\Omega$$

(b) $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$. Therefore,

$$f_r = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6}(10 \text{ k}\Omega)(0.001 \text{ }\mu\text{F})} \cong 6.5 \text{ kHz}$$

- Related Problem** (a) If R_1 , R_2 , and R_3 in Figure 16-14 are changed to 8.2 kΩ, what value must R_f be for oscillation?
- (b) What is the value of f_r ?

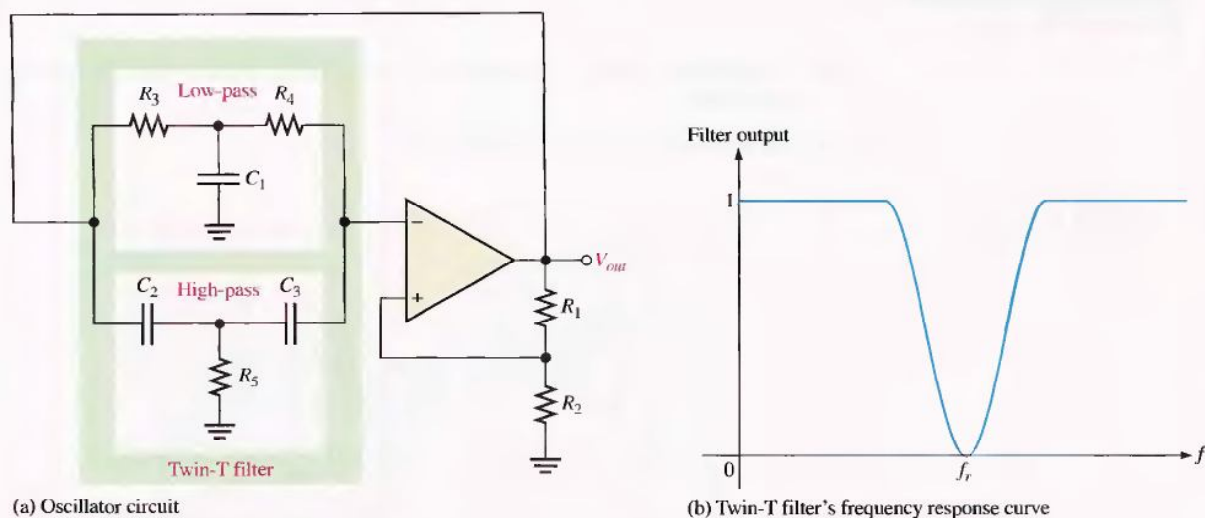


Open the Multisim file E16-02 in the Examples folder on your CD-ROM. Measure the frequency of oscillation and compare to the calculated value.

Twin-T Oscillator

Another type of RC feedback oscillator is called the *twin-T* because of the two T-type RC filters used in the feedback loop, as shown in Figure 16-15(a). One of the twin-T filters has a low-pass response, and the other has a high-pass response. The combined parallel filters produce a band-stop or notch response with a center frequency equal to the desired frequency of oscillation, f_r , as shown in Figure 16-15(b).

Oscillation cannot occur at frequencies above or below f_r because of the negative feedback through the filters. At f_r , however, there is negligible negative feedback; thus, the positive feedback through the voltage divider (R_1 and R_2) allows the circuit to oscillate.



▲ FIGURE 16-15

Twin-T oscillator and twin-T filter response.

SECTION 16-3 REVIEW

1. There are two feedback loops in the Wien-bridge oscillator. What is the purpose of each?
2. A certain lead-lag circuit has $R_1 = R_2$ and $C_1 = C_2$. An input voltage of 5 V rms is applied. The input frequency equals the resonant frequency of the circuit. What is the rms output voltage?
3. Why is the phase shift through the RC feedback circuit in a phase-shift oscillator 180° ?

16-4 OSCILLATORS WITH LC FEEDBACK CIRCUITS

Although the RC feedback oscillators, particularly the Wien bridge, are generally suitable for frequencies up to about 1 MHz, LC feedback elements are normally used in oscillators that require higher frequencies of oscillation. Also, because of the frequency limitation (lower unity-gain frequency) of most op-amps, discrete transistors (BJT or FET) are often used as the gain element in LC oscillators. This section introduces several types of resonant LC feedback oscillators: the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled oscillators.

After completing this section, you should be able to

- Describe and analyze the basic operation of LC feedback oscillators
- Identify and analyze a Colpitts oscillator
- Identify and analyze a Clapp oscillator
- Identify and analyze a Hartley oscillator
- Identify and analyze an Armstrong oscillator
- Discuss the operation of crystal-controlled oscillators

The Colpitts Oscillator

One basic type of resonant circuit feedback oscillator is the Colpitts, named after its inventor—as are most of the others we cover here. As shown in Figure 16–16, this type of oscillator uses an LC circuit in the feedback loop to provide the necessary phase shift and to act as a resonant filter that passes only the desired frequency of oscillation.

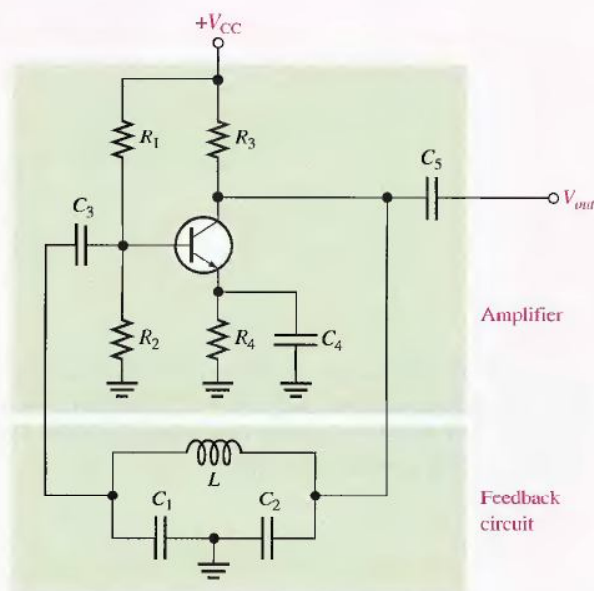


FIGURE 16–16

A basic Colpitts oscillator with a BJT as the gain element.

The approximate frequency of oscillation is the resonant frequency of the LC circuit and is established by the values of C_1 , C_2 , and L according to this familiar formula:

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}}$$

Equation 16–5

where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

Conditions for Oscillation and Start-Up The attenuation, B , of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 and C_2 .

Figure 16–17 shows that the circulating tank current is through both C_1 and C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage (V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (B) is

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)}$$

Cancelling the $2\pi f_r$ terms gives

$$B = \frac{C_2}{C_1}$$

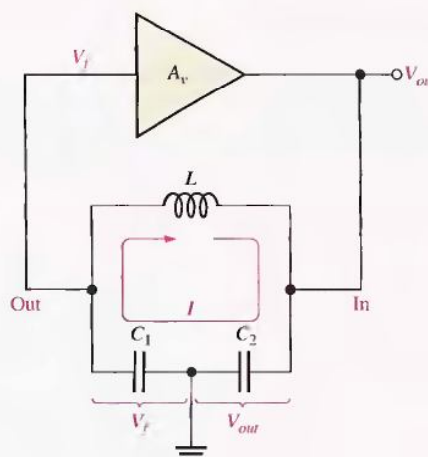
As you know, a condition for oscillation is $A_v B = 1$. Since $B = C_2/C_1$,

$$A_v = \frac{C_1}{C_2}$$

Equation 16–6

► **FIGURE 16-17**

The attenuation of the tank circuit is the output of the tank (V_f) divided by the input to the tank (V_{out}). $B = V_f/V_{out} = C_2/C_1$. For $A_v B > 1$, A_v must be greater than C_1/C_2 .



where A_v is the voltage gain of the amplifier, which is represented by the triangle in Figure 16-17. With this condition met, $A_v B = (C_1/C_2)(C_2/C_1) = 1$. Actually, for the oscillator to be self-starting, $A_v B$ must be greater than 1 (that is, $A_v B > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2 .

$$A_v > \frac{C_1}{C_2}$$

Loading of the Feedback Circuit Affects the Frequency of Oscillation As indicated in Figure 16-18, the input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q of the circuit. Recall from your study of resonance that the resonant frequency of a parallel resonant circuit depends on the Q , according to the following formula:

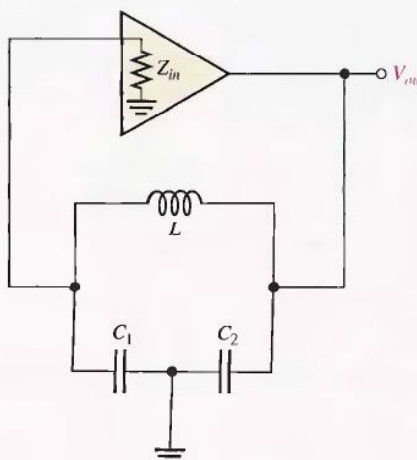
Equation 16-7

$$f_r = \frac{1}{2\pi\sqrt{LC_T}} \sqrt{\frac{Q^2}{Q^2 + 1}}$$

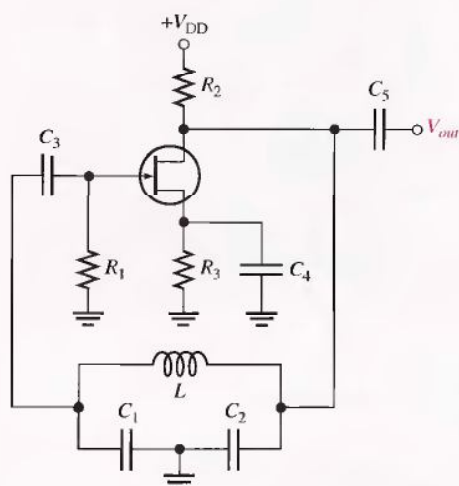
As a rule of thumb, for a Q greater than 10, the frequency is approximately $1/(2\pi\sqrt{LC_T})$, as stated in Equation 16-5. When Q is less than 10, however, f_r is reduced significantly.

► **FIGURE 16-18**

Z_{in} of the amplifier loads the feedback circuit and lowers its Q , thus lowering the resonant frequency.

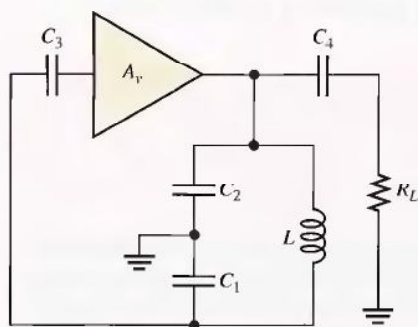


A FET can be used in place of a BJT, as shown in Figure 16–19, to minimize the loading effect of the transistor's input impedance. Recall that FETs have much higher input impedances than do bipolar junction transistors. Also, when an external load is connected to the oscillator output, as shown in Figure 16–20(a), f_r may decrease, again because of a reduction in Q . This happens if the load resistance is too small. In some cases, one way to eliminate the effects of a load resistance is by transformer coupling, as indicated in Figure 16–20(b).

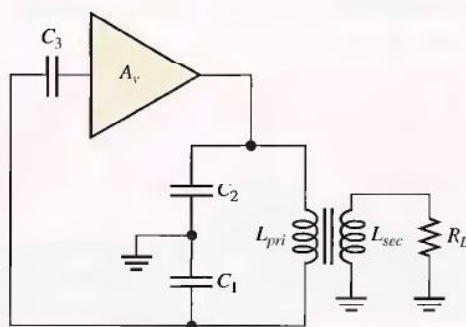


◀ **FIGURE 16–19**

A basic FET Colpitts oscillator.



(a) A load capacitively coupled to oscillator output can reduce circuit Q and f_r .



(b) Transformer coupling of load can reduce loading effect by impedance transformation.

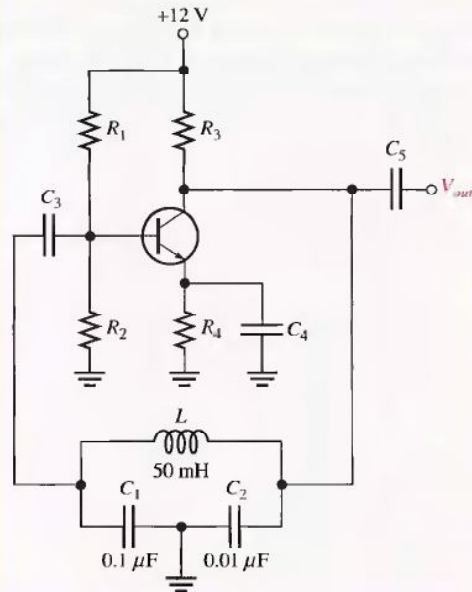
◀ **FIGURE 16–20**

Oscillator loading.

EXAMPLE 16–3

- Determine the frequency for the oscillator in Figure 16–21. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10.
- Find the frequency if the oscillator is loaded to a point where the Q drops to 8.

► FIGURE 16-21



Solution

(a) $C_T = \frac{C_1 C_2}{C_1 + C_2} = \frac{(0.1 \mu\text{F})(0.01 \mu\text{F})}{0.11 \mu\text{F}} = 0.0091 \mu\text{F}$

$f_r \cong \frac{1}{2\pi \sqrt{LC_T}} = \frac{1}{2\pi \sqrt{(50 \text{ mH})(0.0091 \mu\text{F})}} = 7.46 \text{ kHz}$

(b) $f_r = \frac{1}{2\pi \sqrt{LC_T}} \sqrt{\frac{Q^2}{Q^2 + 1}} = (7.46 \text{ kHz})(0.9923) = 7.40 \text{ kHz}$

Related Problem What frequency does the oscillator in Figure 16-21 produce if it is loaded to a point where $Q = 4$?

The Clapp Oscillator

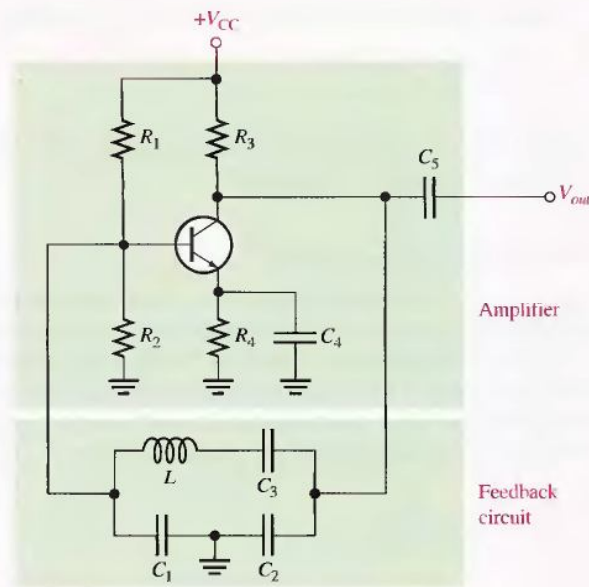
The Clapp oscillator is a variation of the Colpitts. The basic difference is an additional capacitor, C_3 , in series with the inductor in the resonant feedback circuit, as shown in Figure 16-22. Since C_3 is in series with C_1 and C_2 around the tank circuit, the total capacitance is

$$C_T = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

and the approximate frequency of oscillation ($Q > 10$) is

$$f_r \cong \frac{1}{2\pi \sqrt{LC_T}}$$

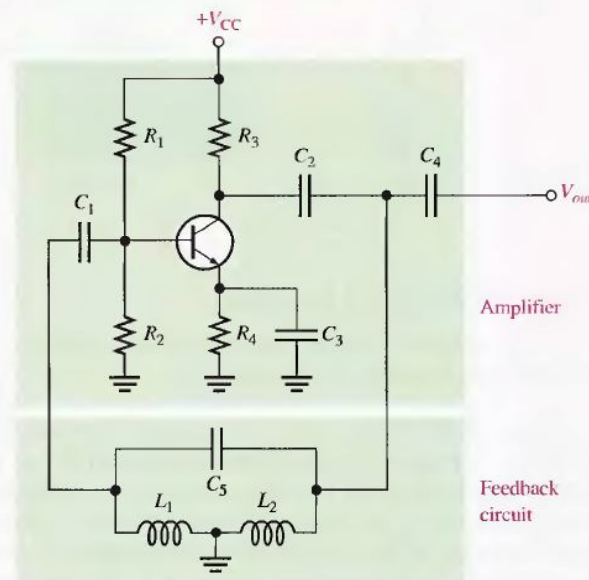
If C_3 is much smaller than C_1 and C_2 , then C_3 almost entirely controls the resonant frequency ($f_r \cong 1/(2\pi \sqrt{LC_3})$). Since C_1 and C_2 are both connected to ground at one end, the junction capacitance of the transistor and other stray capacitances appear in parallel with C_1 and C_2 to ground, altering their effective values. C_3 is not affected, however, and thus provides a more accurate and stable frequency of oscillation.


FIGURE 16-22

A basic Clapp oscillator.

The Hartley Oscillator

The Hartley oscillator is similar to the Colpitts except that the feedback circuit consists of two series inductors and a parallel capacitor as shown in Figure 16-23.


FIGURE 16-23

A basic Hartley oscillator.

In this circuit, the frequency of oscillation for $Q > 10$ is

$$f_r \cong \frac{1}{2\pi\sqrt{L_T C}}$$

where $L_T = L_1 + L_2$. The inductors act in a role similar to C_1 and C_2 in the Colpitts to determine the attenuation, B , of the feedback circuit.

$$B \cong \frac{L_1}{L_2}$$

To assure start-up of oscillation, A_v must be greater than $1/B$.

Equation 16-8

$$A_v > \frac{L_2}{L_1}$$

Loading of the tank circuit has the same effect in the Hartley as in the Colpitts; that is, the Q is decreased and thus f_r decreases.

The Armstrong Oscillator

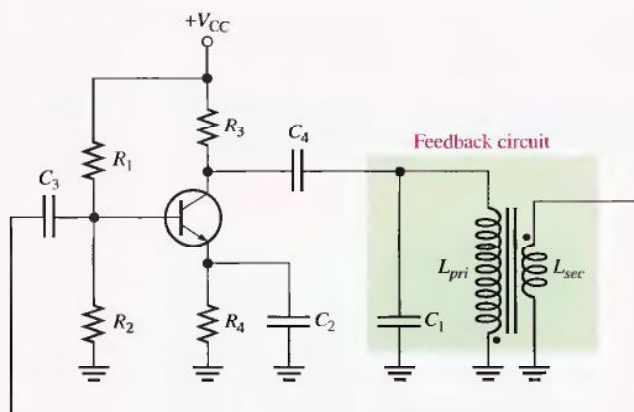
This type of LC feedback oscillator uses transformer coupling to feed back a portion of the signal voltage, as shown in Figure 16-24. It is sometimes called a “tickler” oscillator in reference to the transformer secondary or “tickler coil” that provides the feedback to keep the oscillation going. The Armstrong is less common than the Colpitts, Clapp, and Hartley, mainly because of the disadvantage of transformer size and cost. The frequency of oscillation is set by the inductance of the primary winding (L_{pri}) in parallel with C_1 .

Equation 16-9

$$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}}$$

► FIGURE 16-24

A basic Armstrong oscillator.



Crystal-Controlled Oscillators

The most stable and accurate type of feedback oscillator uses a piezoelectric **crystal** in the feedback loop to control the frequency.

The Piezoelectric Effect Quartz is one type of crystalline substance found in nature that exhibits a property called the **piezoelectric effect**. When a changing mechanical stress is applied across the crystal to cause it to vibrate, a voltage develops at the frequency of mechanical vibration. Conversely, when an ac voltage is applied across the crystal, it vibrates at the frequency of the applied voltage. The greatest vibration occurs at the crystal's natural resonant frequency, which is determined by the physical dimensions and by the way the crystal is cut.

Crystals used in electronic applications typically consist of a quartz wafer mounted between two electrodes and enclosed in a protective “can” as shown in Figure 16-25(a) and (b). A schematic symbol for a crystal is shown in Figure 16-25(c), and an equivalent RLC circuit for the crystal appears in Figure 16-25(d). As you can see, the crystal's equivalent circuit is a series-parallel RLC circuit and can operate in either series resonance or parallel resonance. At the series resonant frequency, the inductive reactance is cancelled by the reactance of C_s . The remaining series resistor, R_s , determines the impedance of the crystal. Parallel resonance occurs when the inductive reactance and the reactance of the parallel capacitance, C_m , are equal. The parallel resonant frequency is usually at least 1 kHz higher

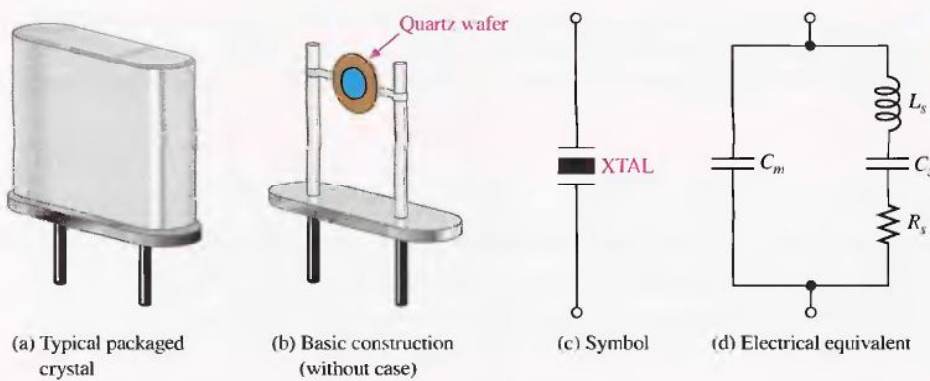


FIGURE 16-25

A quartz crystal.

than the series resonant frequency. A great advantage of the crystal is that it exhibits a very high Q (Q s with values of several thousand are typical).

An oscillator that uses a crystal as a series resonant tank circuit is shown in Figure 16-26(a). The impedance of the crystal is minimum at the series resonant frequency, thus providing maximum feedback. The crystal tuning capacitor, C_C , is used to “fine tune” the oscillator frequency by “pulling” the resonant frequency of the crystal slightly up or down.

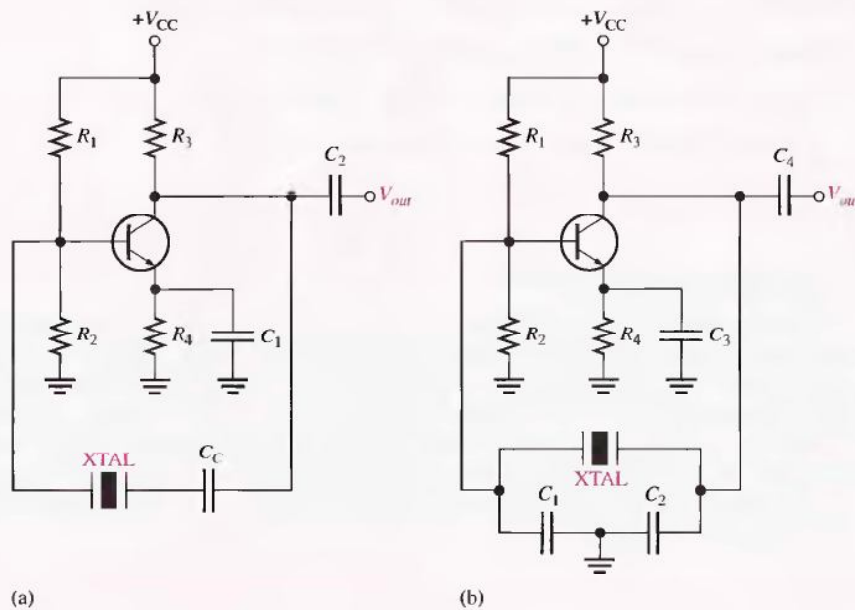


FIGURE 16-26

Basic crystal oscillators.

A modified Colpitts configuration is shown in Figure 16-26(b) with a crystal acting as a parallel resonant tank circuit. The impedance of the crystal is maximum at parallel resonance, thus developing the maximum voltage across the capacitors. The voltage across C_1 is fed back to the input.

Modes of Oscillation in the Crystal Piezoelectric crystals can oscillate in either of two modes—fundamental or overtone. The fundamental frequency of a crystal is the lowest frequency at which it is naturally resonant. The fundamental frequency depends on the crystal’s mechanical dimensions, type of cut, and other factors, and is inversely proportional to the thickness of the crystal slab. Because a slab of crystal cannot be cut too thin without fracturing, there is an upper limit on the fundamental frequency. For most crystals, this upper limit

is less than 20 MHz. For higher frequencies, the crystal must be operated in the overtone mode. Overtones are approximate integer multiples of the fundamental frequency. The overtone frequencies are usually, but not always, odd multiples (3, 5, 7, . . .) of the fundamental.

SECTION 16-4 REVIEW

1. What is the basic difference between the Colpitts and the Hartley oscillators?
2. What is the advantage of a FET amplifier in a Colpitts or Hartley oscillator?
3. How can you distinguish a Colpitts oscillator from a Clapp oscillator?

16-5 RELAXATION OSCILLATORS

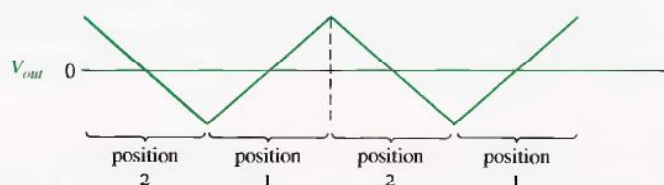
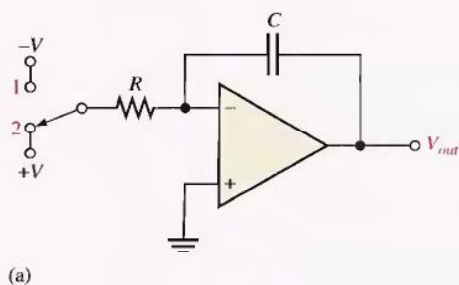
The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an RC timing circuit and a device that changes states to generate a periodic waveform. In this section, you will learn about several circuits that are used to produce nonsinusoidal waveforms.

After completing this section, you should be able to

- Describe and analyze the basic operation of relaxation oscillators
- Discuss the operation of basic triangular-wave oscillators
- Discuss the operation of a voltage-controlled oscillator (VCO)
- Discuss the operation of a square-wave relaxation oscillator

A Triangular-Wave Oscillator

The op-amp integrator covered in Chapter 13 can be used as the basis for a triangular-wave oscillator. The basic idea is illustrated in Figure 16-27(a) where a dual-polarity, switched input is used. We use the switch only to introduce the concept; it is not a practical way to implement this circuit. When the switch is in position 1, the negative voltage is applied, and the output is a positive-going ramp. When the switch is thrown into position 2, a negative-going ramp is produced. If the switch is thrown back and forth at fixed intervals, the output is a triangular wave consisting of alternating positive-going and negative-going ramps, as shown in Figure 16-27(b).



▲ FIGURE 16-27

Basic triangular-wave oscillator.

A Practical Triangular-Wave Oscillator One practical implementation of a triangular-wave oscillator utilizes an op-amp comparator to perform the switching function, as shown in Figure 16-28. The operation is as follows. To begin, assume that the output voltage of the comparator is at its maximum negative level. This output is connected to the inverting input of the integrator through R_1 , producing a positive-going ramp on the output of the integrator. When the ramp voltage reaches the upper trigger point (UTP), the comparator switches to its maximum positive level. This positive level causes the integrator ramp to change to a negative-going direction. The ramp continues in this direction until the lower trigger point (LTP) of the comparator is reached. At this point, the comparator output switches back to the maximum negative level and the cycle repeats. This action is illustrated in Figure 16-29.

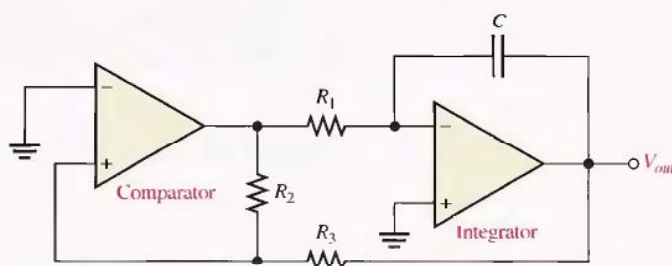


FIGURE 16-28

A triangular-wave oscillator using two op-amps.

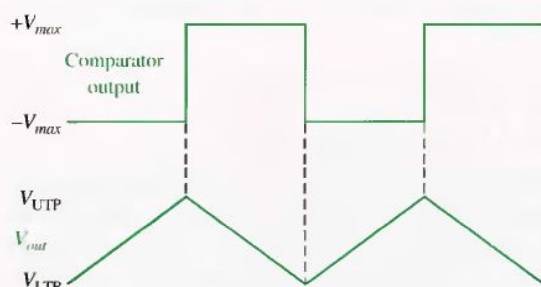


FIGURE 16-29

Waveforms for the circuit in Figure 16-28.

Since the comparator produces a square-wave output, the circuit in Figure 16-28 can be used as both a triangular-wave oscillator and a square-wave oscillator. Devices of this type are commonly known as *function generators* because they produce more than one output function. The output amplitude of the square wave is set by the output swing of the comparator, and the resistors R_2 and R_3 set the amplitude of the triangular output by establishing the UTP and LTP voltages according to the following formulas:

$$V_{UTP} = +V_{max} \left(\frac{R_3}{R_2} \right)$$

$$V_{LTP} = -V_{max} \left(\frac{R_3}{R_2} \right)$$

where the comparator output levels, $+V_{max}$ and $-V_{max}$, are equal. The frequency of both waveforms depends on the R_1C time constant as well as the amplitude-setting resistors, R_2 and R_3 . By varying R_1 , the frequency of oscillation can be adjusted without changing the output amplitude.

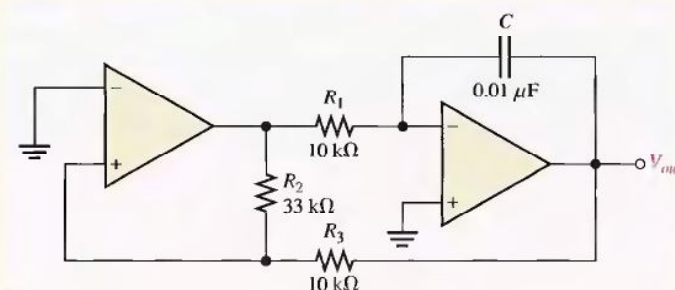
$$f_r = \frac{1}{4R_1C} \left(\frac{R_2}{R_3} \right)$$

Equation 16-10

EXAMPLE 16-4

Determine the frequency of oscillation of the circuit in Figure 16-30. To what value must R_1 be changed to make the frequency 20 kHz?

► **FIGURE 16-30**



Solution

$$f_r = \frac{1}{4R_1C} \left(\frac{R_2}{R_3} \right) = \left(\frac{1}{4(10 \text{ k}\Omega)(0.01 \text{ }\mu\text{F})} \right) \left(\frac{33 \text{ k}\Omega}{10 \text{ k}\Omega} \right) = 8.25 \text{ kHz}$$

To make $f = 20 \text{ kHz}$,

$$R_1 = \frac{1}{4fC} \left(\frac{R_2}{R_3} \right) = \left(\frac{1}{4(20 \text{ kHz})(0.01 \text{ }\mu\text{F})} \right) \left(\frac{33 \text{ k}\Omega}{10 \text{ k}\Omega} \right) = 4.13 \text{ k}\Omega$$

Related Problem

What is the amplitude of the triangular wave in Figure 16-30 if the comparator output is $\pm 10 \text{ V}$?

A Sawtooth Voltage-Controlled Oscillator (VCO)



The **voltage-controlled oscillator (VCO)** is a relaxation oscillator whose frequency can be changed by a variable dc control voltage. VCOs can be either sinusoidal or nonsinusoidal. One way to build a sawtooth VCO is with an op-amp integrator that uses a switching device (PUT) in parallel with the feedback capacitor to terminate each ramp at a prescribed level and effectively “reset” the circuit. Figure 16-31(a) shows the implementation.

As you learned in Chapter 11, the PUT is a programmable unijunction transistor with an anode, a cathode, and a gate terminal. The gate is always biased positively with respect to the cathode. When the anode voltage exceeds the gate voltage by approximately 0.7 V, the PUT turns on and acts as a forward-biased diode. When the anode voltage falls below this level, the PUT turns off. Also, the current must be above the holding value to maintain conduction.

The operation of the sawtooth VCO begins when the negative dc input voltage, $-V_{IN}$, produces a positive-going ramp on the output. During the time that the ramp is increasing, the circuit acts as a regular integrator. The PUT triggers on when the output ramp (at the anode) exceeds the gate voltage by 0.7 V. The gate is set to the approximate desired sawtooth peak voltage. When the PUT turns on, the capacitor rapidly discharges, as shown in Figure 16-31(b). The capacitor does not discharge completely to zero because of the PUT’s forward voltage, V_F . Discharge continues until the PUT current falls below the holding value. At this point, the PUT turns off and the capacitor begins to charge again, thus generating a new output ramp. The cycle continually repeats, and the resulting output is a repetitive sawtooth waveform, as shown. The sawtooth amplitude and period can be adjusted by varying the PUT gate voltage.

The frequency of oscillation is determined by the R_iC time constant of the integrator and the peak voltage set by the PUT. Recall that the charging rate of a capacitor is V_{IN}/R_iC . The time it takes a capacitor to charge from V_F to V_p is the period, T , of the sawtooth waveform (neglecting the rapid discharge time).

$$T = \frac{V_p - V_F}{|V_{IN}|/R_iC}$$

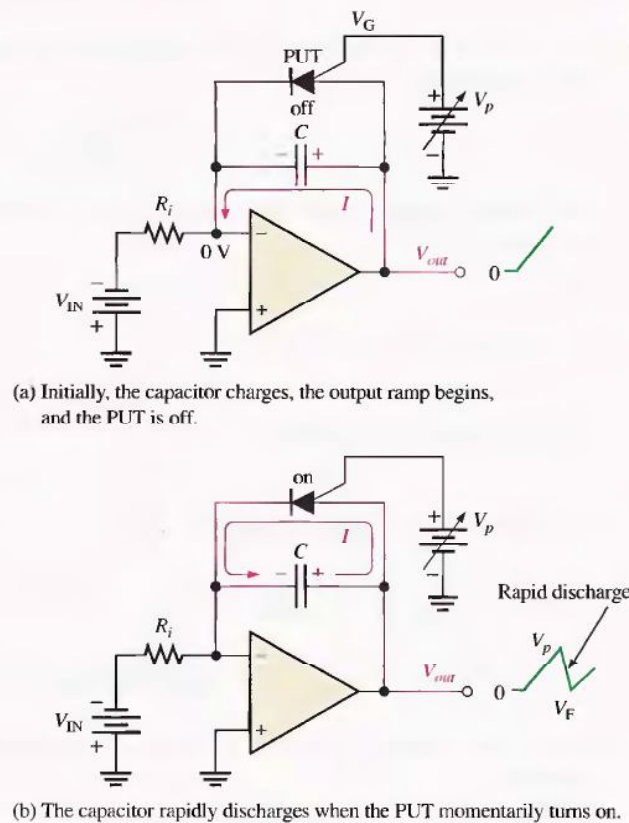


FIGURE 16-31
Sawtooth VCO operation.

From $f = 1/T$,

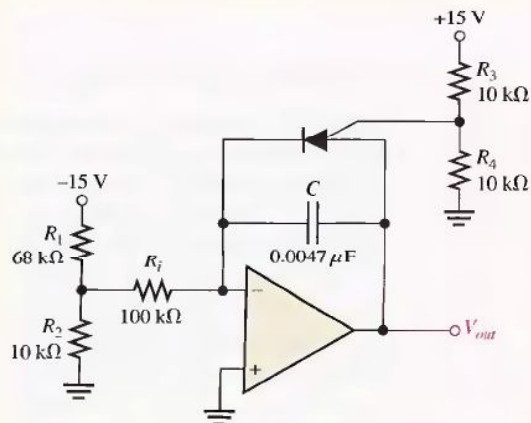
$$f = \frac{|V_{IN}|}{R_i C} \left(\frac{1}{V_p - V_F} \right)$$

Equation 16-11

EXAMPLE 16-5

- Find the amplitude and frequency of the sawtooth output in Figure 16-32. Assume that the forward PUT voltage, V_F , is approximately 1 V.
- Sketch the output waveform.

FIGURE 16-32



- Solution** (a) First, find the gate voltage in order to establish the approximate voltage at which the PUT turns on.

$$V_G = \frac{R_4}{R_3 + R_4} (+V) = \frac{10 \text{ k}\Omega}{20 \text{ k}\Omega} (15 \text{ V}) = 7.5 \text{ V}$$

This voltage sets the approximate maximum peak value of the sawtooth output (neglecting the 0.7 V).

$$V_p \cong 7.5 \text{ V}$$

The minimum peak value (low point) is

$$V_F \cong 1 \text{ V}$$

So the peak-to-peak amplitude is

$$V_{pp} = V_p - V_F = 7.5 \text{ V} - 1 \text{ V} = 6.5 \text{ V}$$

The frequency is determined as follows:

$$V_{IN} = \frac{R_2}{R_1 + R_2} (-V) = \frac{10 \text{ k}\Omega}{78 \text{ k}\Omega} (-15 \text{ V}) = -1.92 \text{ V}$$

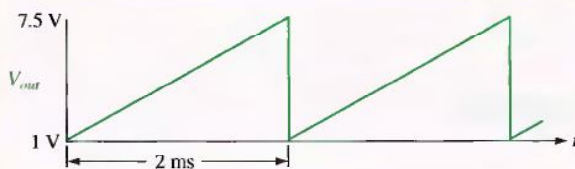
$$f = \frac{|V_{IN}|}{R_i C} \left(\frac{1}{V_p - V_F} \right) = \left(\frac{1.92 \text{ V}}{(100 \text{ k}\Omega)(0.0047 \text{ }\mu\text{F})} \right) \left(\frac{1}{7.5 \text{ V} - 1 \text{ V}} \right) = 628 \text{ Hz}$$

- (b) The output waveform is shown in Figure 16-33, where the period is determined as follows:

$$T = \frac{1}{f} = \frac{1}{628 \text{ Hz}} = 2 \text{ ms}$$

► **FIGURE 16-33**

Output of the circuit in Figure 16-32.



Related Problem If R_i is changed to 56 k Ω in Figure 16-32, what is the frequency?

A Square-Wave Oscillator

The basic square-wave oscillator shown in Figure 16-34 is a type of relaxation oscillator because its operation is based on the charging and discharging of a capacitor. Notice that the op-amp's inverting input is the capacitor voltage and the noninverting input is a portion of the output fed back through resistors R_2 and R_3 . When the circuit is first turned on, the capacitor is uncharged, and thus the inverting input is at 0 V. This makes the output a positive maximum, and the capacitor begins to charge toward V_{out} through R_1 . When the capacitor voltage (V_C) reaches a value equal to the feedback voltage (V_F) on the noninverting input, the op-amp switches to the maximum negative state. At this point, the capacitor begins to discharge from $+V_f$ toward $-V_f$. When the capacitor voltage reaches $-V_f$, the op-amp switches back to the maximum positive state. This action continues to repeat, as shown in Figure 16-35, and a square-wave output voltage is obtained.

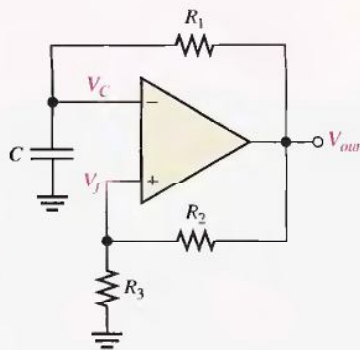


FIGURE 16-34

A square-wave relaxation oscillator.

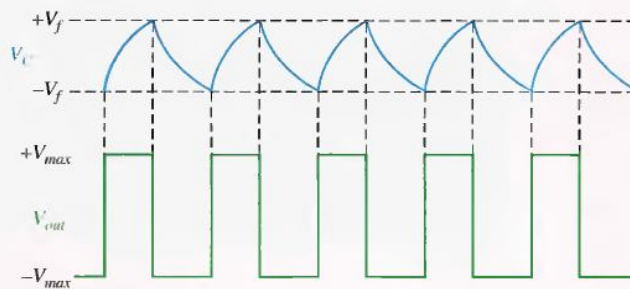


FIGURE 16-35

Waveforms for the square-wave relaxation oscillator.

SECTION 16-5 REVIEW

1. What is a VCO, and basically, what does it do?
2. Upon what principle does a relaxation oscillator operate?

16-6 THE 555 TIMER AS AN OSCILLATOR

The 555 timer is a versatile integrated circuit with many applications. In this section, you will see how the 555 is configured as an astable or free-running multivibrator, which is essentially a square-wave oscillator. The use of the 555 timer as a voltage-controlled oscillator (VCO) is also discussed.

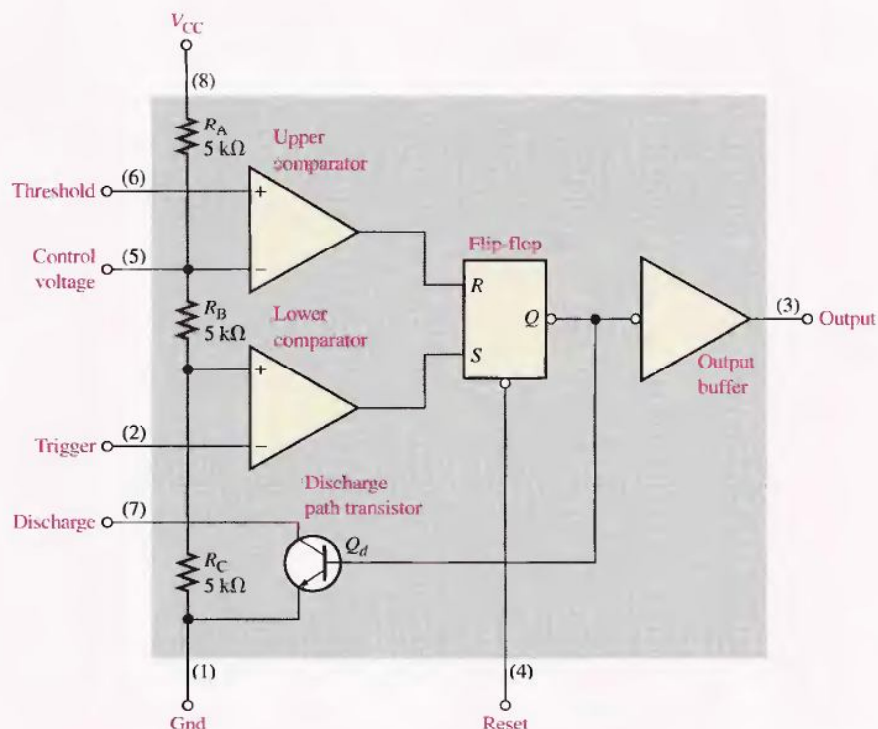
After completing this section, you should be able to

- Use a 555 timer in an oscillator application
- Explain what the 555 timer is
- Discuss astable operation of the 555 timer
- Explain how to use the 555 timer as a VCO

The 555 timer consists basically of two comparators, a flip-flop, a discharge transistor, and a resistive voltage divider, as shown in Figure 16-36. The flip-flop (bistable multivibrator) is a digital device that may be unfamiliar to you at this point unless you already have taken a digital fundamentals course. Briefly, it is a two-state device whose output can be at either a high voltage level (set, S) or a low voltage level (reset, R). The state of the output can be changed with proper input signals.

► FIGURE 16-36

Internal diagram of a 555 integrated circuit timer. (IC pin numbers are in parentheses.)



The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value; therefore, the upper comparator has a reference of $\frac{2}{3}V_{CC}$, and the lower comparator has a reference of $\frac{1}{3}V_{CC}$. The comparators' outputs control the state of the flip-flop. When the trigger voltage goes below $\frac{1}{3}V_{CC}$, the flip-flop sets and the output jumps to its high level. The threshold input is normally connected to an external RC timing circuit. When the external capacitor voltage exceeds $\frac{2}{3}V_{CC}$, the upper comparator resets the flip-flop, which in turn switches the output back to its low level. When the device output is low, the discharge transistor (Q_d) is turned on and provides a path for rapid discharge of the external timing capacitor. This basic operation allows the timer to be configured with external components as an oscillator, a one-shot, or a time-delay element.

Astable Operation

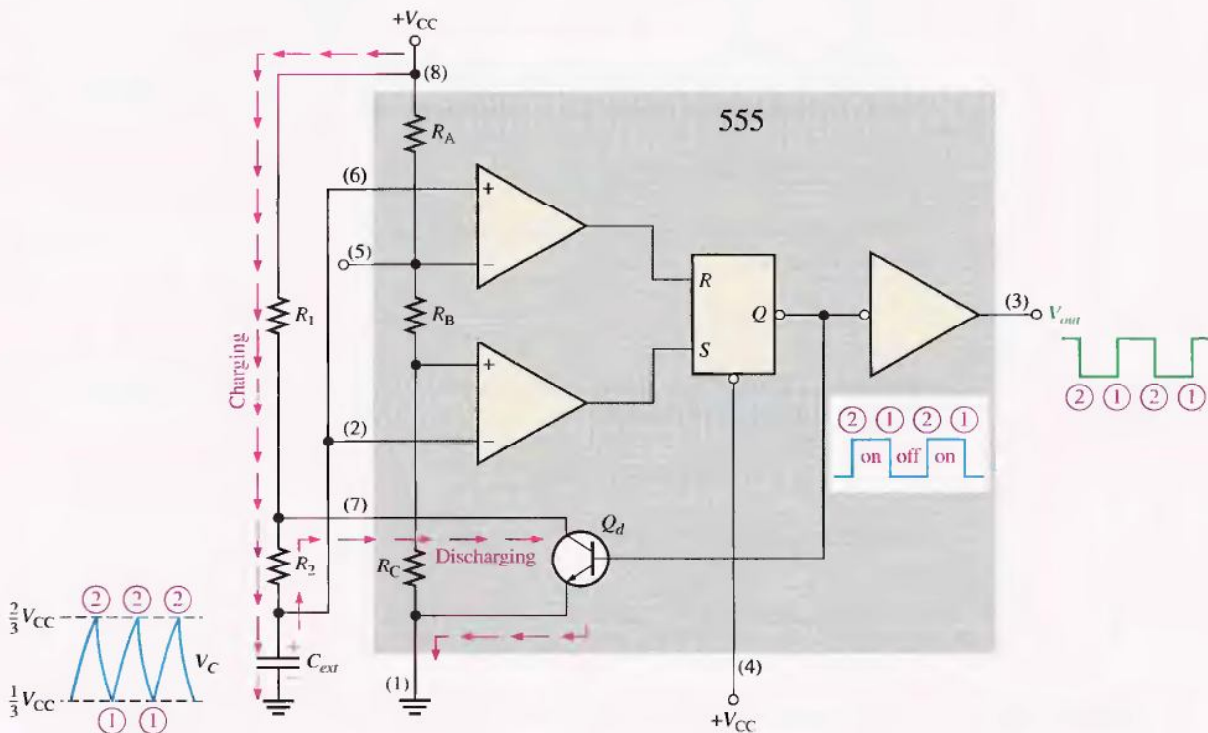
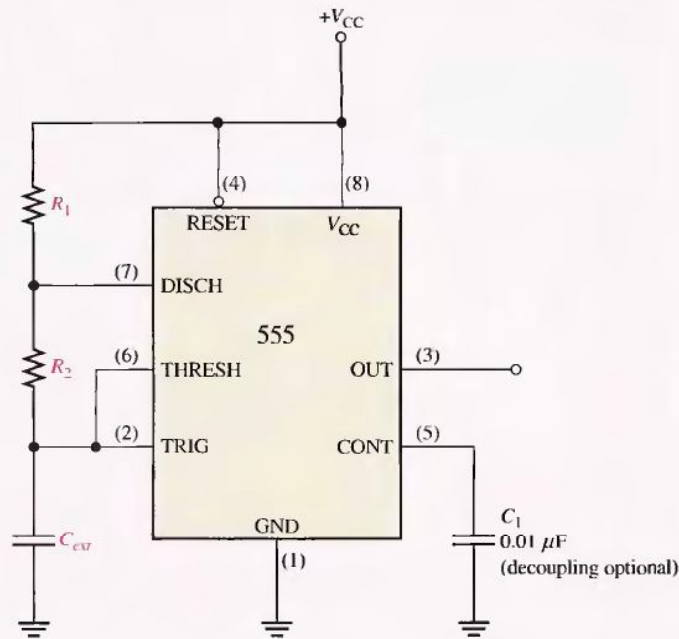


A 555 timer connected to operate in the **astable** mode as a free-running relaxation oscillator (astable multivibrator) is shown in Figure 16-37. Notice that the threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1 , R_2 , and C_{ext} form the timing circuit that sets the frequency of oscillation. The $0.01 \mu\text{F}$ capacitor connected to the control (CONT) input is strictly for decoupling and has no effect on the operation.

Initially, when the power is turned on, the capacitor C_{ext} is uncharged and thus the trigger voltage (pin 2) is at 0 V. This causes the output of the lower comparator to be high and the output of the upper comparator to be low, forcing the output of the flip-flop, and thus the base of Q_d , low and keeping the transistor off. Now, C_{ext} begins charging through R_1 and R_2 as indicated in Figure 16-38. When the capacitor voltage reaches $\frac{1}{3}V_{CC}$, the lower comparator switches to its low output state, and when the capacitor voltage reaches $\frac{2}{3}V_{CC}$, the upper comparator switches to its high output state. This resets the flip-flop, causes the base of Q_d to go high, and turns on the transistor. This sequence creates a discharge path for the capacitor through R_2 and the transistor, as indicated. The capacitor now begins to discharge, causing the upper comparator to go low. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, the lower comparator switches high, setting the flip-flop, which makes the base of Q_d low and turns off the transistor. Another charging cycle begins, and the entire process

◀ FIGURE 16-37

The 555 timer connected as an astable multivibrator.



▲ FIGURE 16-38

Operation of the 555 timer in the astable mode.

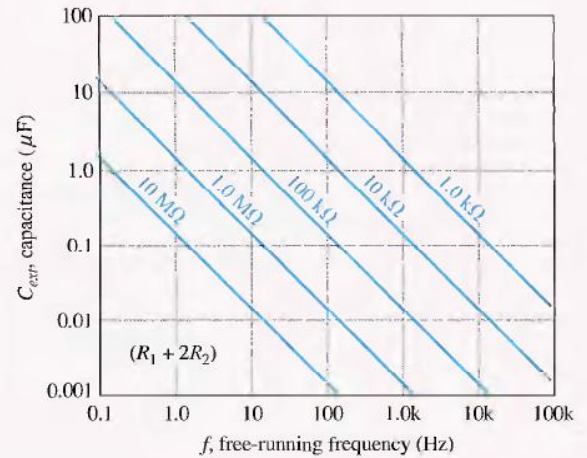
repeats. The result is a rectangular wave output whose duty cycle depends on the values of R_1 and R_2 . The frequency of oscillation is given by Equation 16-12, or it can be found using the graph in Figure 16-39.

$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$$

Equation 16-12

FIGURE 16-39

Frequency of oscillation (free-running frequency) of a 555 timer in the astable mode as a function of C_{ext} and $R_1 + 2R_2$. The sloped lines are values of $R_1 + 2R_2$.



By selecting R_1 and R_2 , the duty cycle of the output can be adjusted. Since C_{ext} charges through $R_1 + R_2$ and discharges only through R_2 , duty cycles approaching a minimum of 50 percent can be achieved if $R_2 \gg R_1$ so that the charging and discharging times are approximately equal.

A formula to calculate the duty cycle is developed as follows. The time that the output is high (t_H) is how long it takes C_{ext} to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$. It is expressed as

$$t_H = 0.694(R_1 + R_2)C_{ext}$$

The time that the output is low (t_L) is how long it takes C_{ext} to discharge from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$. It is expressed as

$$t_L = 0.694R_2C_{ext}$$

The period, T , of the output waveform is the sum of t_H and t_L . The following formula for T is the reciprocal of f in Equation 16-12.

$$T = t_H + t_L = 0.694(R_1 + 2R_2)C_{ext}$$

Finally, the percent duty cycle is

$$\text{Duty cycle} = \left(\frac{t_H}{T} \right) 100\% = \left(\frac{t_H}{t_H + t_L} \right) 100\%$$

Equation 16-13

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\%$$

To achieve duty cycles of less than 50 percent, the circuit in Figure 16-37 can be modified so that C_{ext} charges through only R_1 and discharges through R_2 . This is achieved with a diode, D_1 , placed as shown in Figure 16-40. The duty cycle can be made less than 50 percent by making R_1 less than R_2 . Under this condition, the formula for the percent duty cycle is

Equation 16-14

$$\text{Duty cycle} = \left(\frac{R_1}{R_1 + R_2} \right) 100\%$$

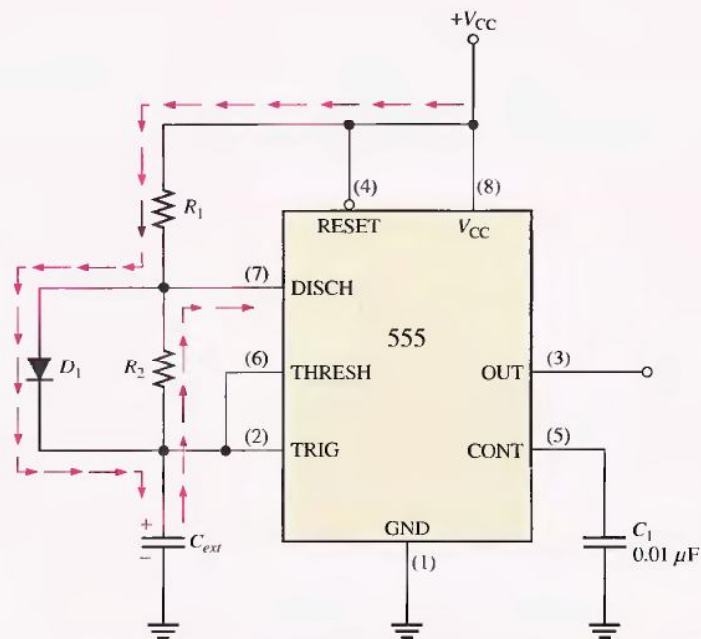


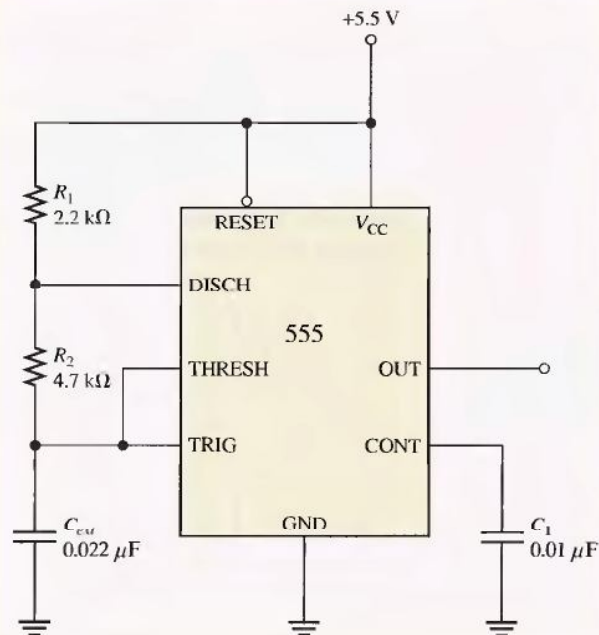
FIGURE 16-40

The addition of diode D_1 allows the duty cycle of the output to be adjusted to less than 50 percent by making $R_1 < R_2$.

EXAMPLE 16-6

A 555 timer configured to run in the astable mode (oscillator) is shown in Figure 16-41. Determine the frequency of the output and the duty cycle.

FIGURE 16-41

**Solution**

$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}} = \frac{1.44}{(2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega)0.022 \text{ }\mu\text{F}} = 5.64 \text{ kHz}$$

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\% = \left(\frac{2.2 \text{ k}\Omega + 4.7 \text{ k}\Omega}{2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega} \right) 100\% = 59.5\%$$

Related Problem

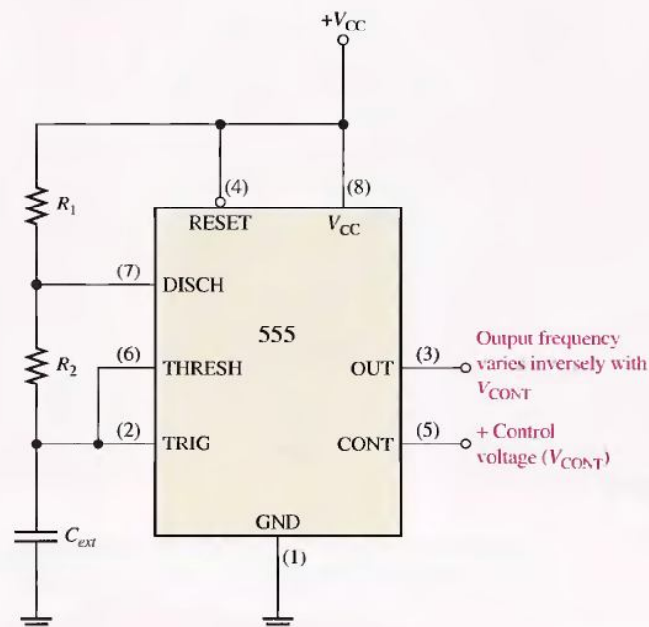
Determine the duty cycle in Figure 16-41 if a diode is connected across R_2 as indicated in Figure 16-40.

Operation as a Voltage-Controlled Oscillator (VCO)

A 555 timer can be set up to operate as a VCO by using the same external connections as for astable operation, with the exception that a variable control voltage is applied to the CONT input (pin 5), as indicated in Figure 16-42.

► **FIGURE 16-42**

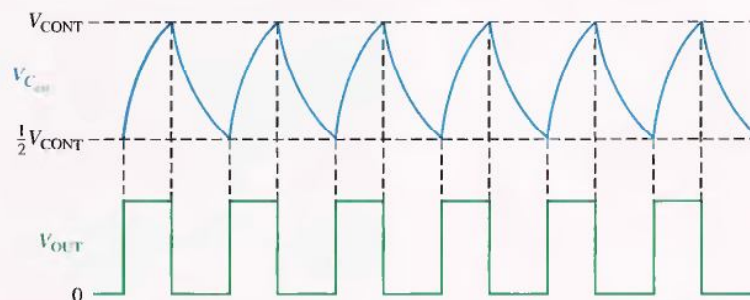
The 555 timer connected as a voltage-controlled oscillator (VCO). Note the variable control voltage input on pin 5.



As shown in Figure 16-43, the control voltage (V_{CONT}) changes the threshold values of $\frac{1}{2}V_{\text{CC}}$ and $\frac{2}{3}V_{\text{CC}}$ for the internal comparators. With the control voltage, the upper value is V_{CONT} and the lower value is $\frac{1}{2}V_{\text{CONT}}$, as you can see by examining the internal diagram of the 555 timer. When the control voltage is varied, the output frequency also varies. An increase in V_{CONT} increases the charging and discharging time of the external capacitor and causes the frequency to decrease. A decrease in V_{CONT} decreases the charging and discharging time of the capacitor and causes the frequency to increase.

► **FIGURE 16-43**

The VCO output frequency varies inversely with V_{CONT} because the charging and discharging time of C_{ext} is directly dependent on the control voltage.



An interesting application of the VCO is in phase-locked loops, which are used in various types of communication receivers to track variations in the frequency of incoming signals. You will learn about the basic operation of a phase-locked loop in Section 17-8.

SECTION 16-6 REVIEW

1. Name the five basic elements in a 555 timer IC.
2. When the 555 timer is configured as an astable multivibrator, how is the duty cycle determined?



SYSTEM APPLICATION

This system application focuses on a function generator, an instrument that produces sinusoidal waveforms, square waveforms, and triangular waveforms for use in testing circuits in the laboratory.

Basic Operation of the System

The function generator is an electronic system that produces either a sinusoidal waveform, a square waveform, or a triangular waveform depending on the function selected by the front panel switches, as shown in Figure 16-44. The frequency of the selected output waveform can be varied from less than 1 Hz to greater than 80 kHz by using the frequency range switches and the frequency dial. The amplitude of the output waveform can be adjusted up to approximately +10 V with the front panel amplitude control. Also, any dc offset can be nulled out with the front panel dc offset control.

The block diagram of the function generator is shown in Figure 16-45.

The concept of this particular design is simple. The oscillator produces a sinusoidal output voltage that drives a zero-level detector (comparator), which produces a square wave of the same frequency as the oscillator output. The output of the level detector goes to an integrator, which produces a triangular output voltage also with a frequency equal to the oscillator output. The type of output waveform is selected by the function switches on the front panel. The frequency is set by the front panel range switches and the frequency dial, and amplitude is set by the front panel control knob.

The schematic of the function generator is shown in Figure 16-46, where



FIGURE 16-44
Front panel of the function generator.

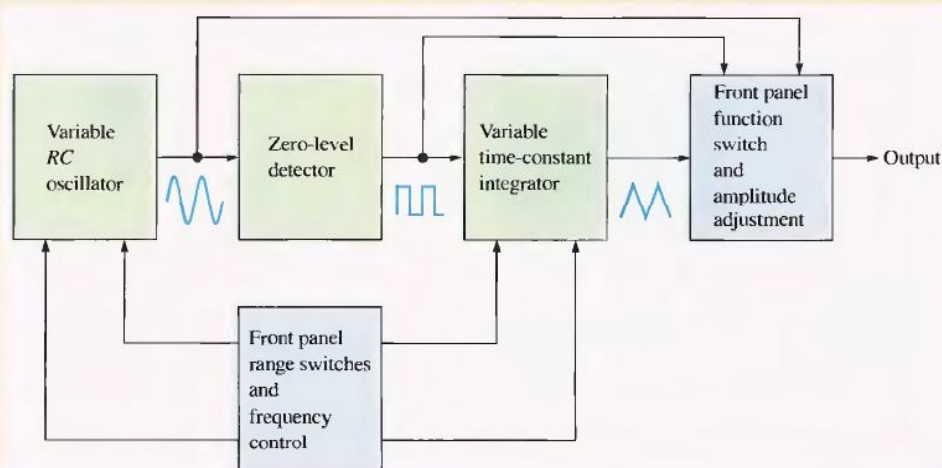


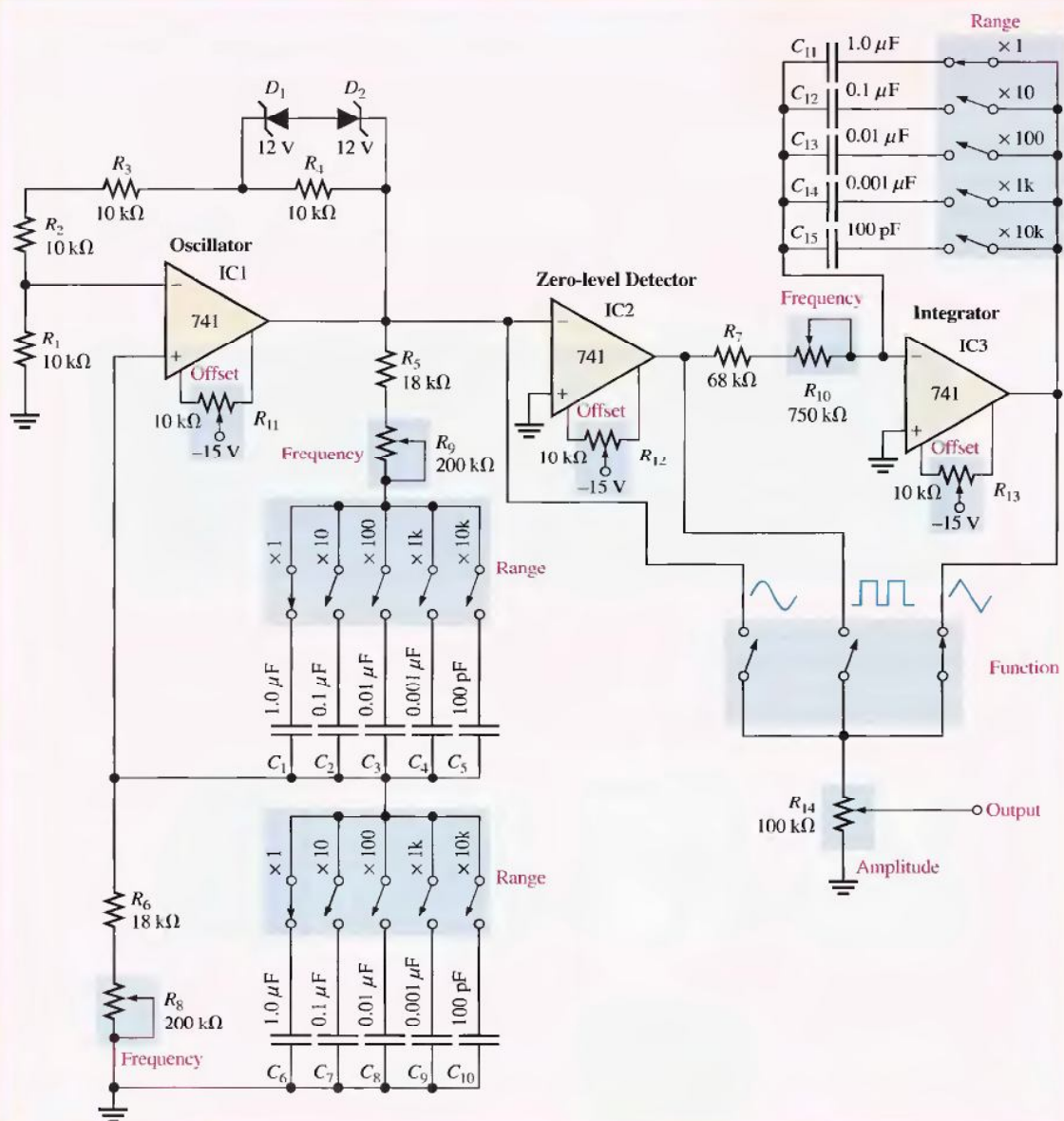
FIGURE 16-45
Block diagram of the function generator.

the portions in blue are the front panel components. The frequency of the sinusoidal oscillator is controlled by the selection of any two of ten capacitors (C_1 through C_{10}) in the oscillator feedback circuit. These capacitors produce the five frequency ranges indicated on the front panel switches, which are multiplication factors for the setting of the frequency

dial. The adjustment of the frequency within each range is accomplished by varying resistors R_8 and R_9 in the feedback circuit of the oscillator.

The integrator time constant is adjusted in step with the frequency by selection of the appropriate capacitor (C_{11} through C_{15}) and adjustment of resistor R_{10} . Resistors R_8 , R_9 , and R_{10} are poten-

tiometers that are ganged together so that they change resistance together as the frequency dial is turned. For example, if the $\times 1k$ switch is selected and the frequency dial is set at 5, then the resulting output frequency for any of the three types of waveforms is $1 \text{ kHz} \times 5 = 5 \text{ kHz}$.



▲ FIGURE 16-46

Schematic of the function generator.

The Function Generator Circuit Boards

- Make sure that the circuit boards shown in Figure 16–47 are correct by checking them against the schematic in Figure 16–46. Backside interconnections are shown as darker traces.
- Label a copy of the board with component and input/output designations in agreement with the schematic.
- Develop a board-to-board wire list specifying which terminals on the two boards connect together and which terminals connect to front panel components.

The Function Generator Circuit

- Determine the maximum frequency of the oscillator for each range switch ($\times 1$,

$\times 10$, $\times 100$, $\times 1k$, and $\times 10k$). Only one set of three switches corresponding to a given range setting can be closed at a time. There is a set of ganged switches for $\times 1$, a set of ganged switches for $\times 10$, and so on.

- Determine the minimum frequency of the oscillator for each range switch.
- Determine the approximate maximum peak-to-peak output voltages for each function. The dc supply voltages are $+15\text{ V}$ and -15 V .

Test Procedure

Develop a basic procedure for thoroughly testing the function generator.

Troubleshooting

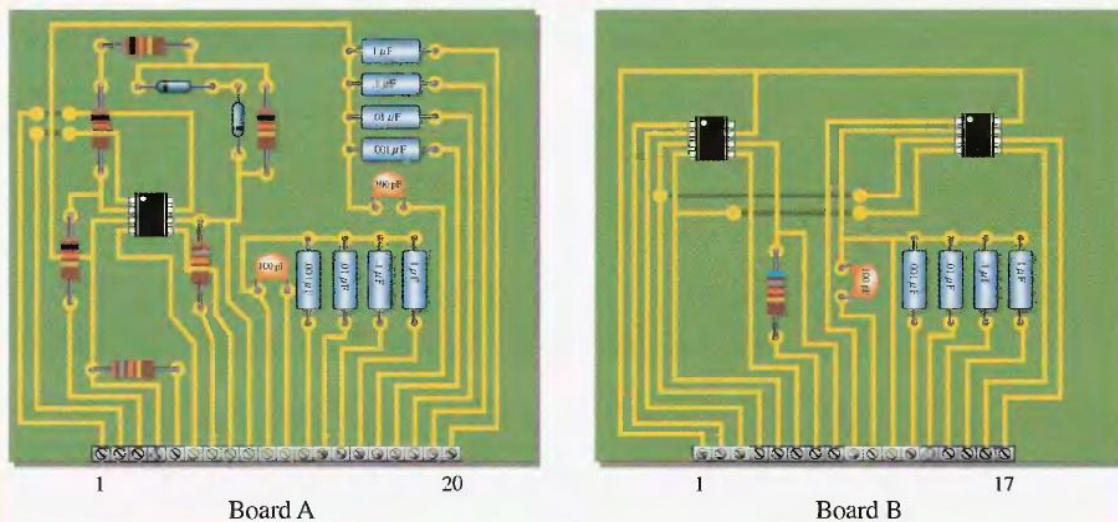
Based on the results indicated in Figure 16–48 for four faulty function generator

units, determine the most likely fault or faults in each case.

Final Report (Optional)

Submit a final written report on the channel filter boards using an organized format that includes the following:

1. A physical description of the circuit.
2. A discussion of the operation of the circuit.
3. A list of the specifications.
4. A list of parts with part numbers if available.
5. A list of the types of problems in the four faulty units.



▲ FIGURE 16–47

The function generator circuit boards.

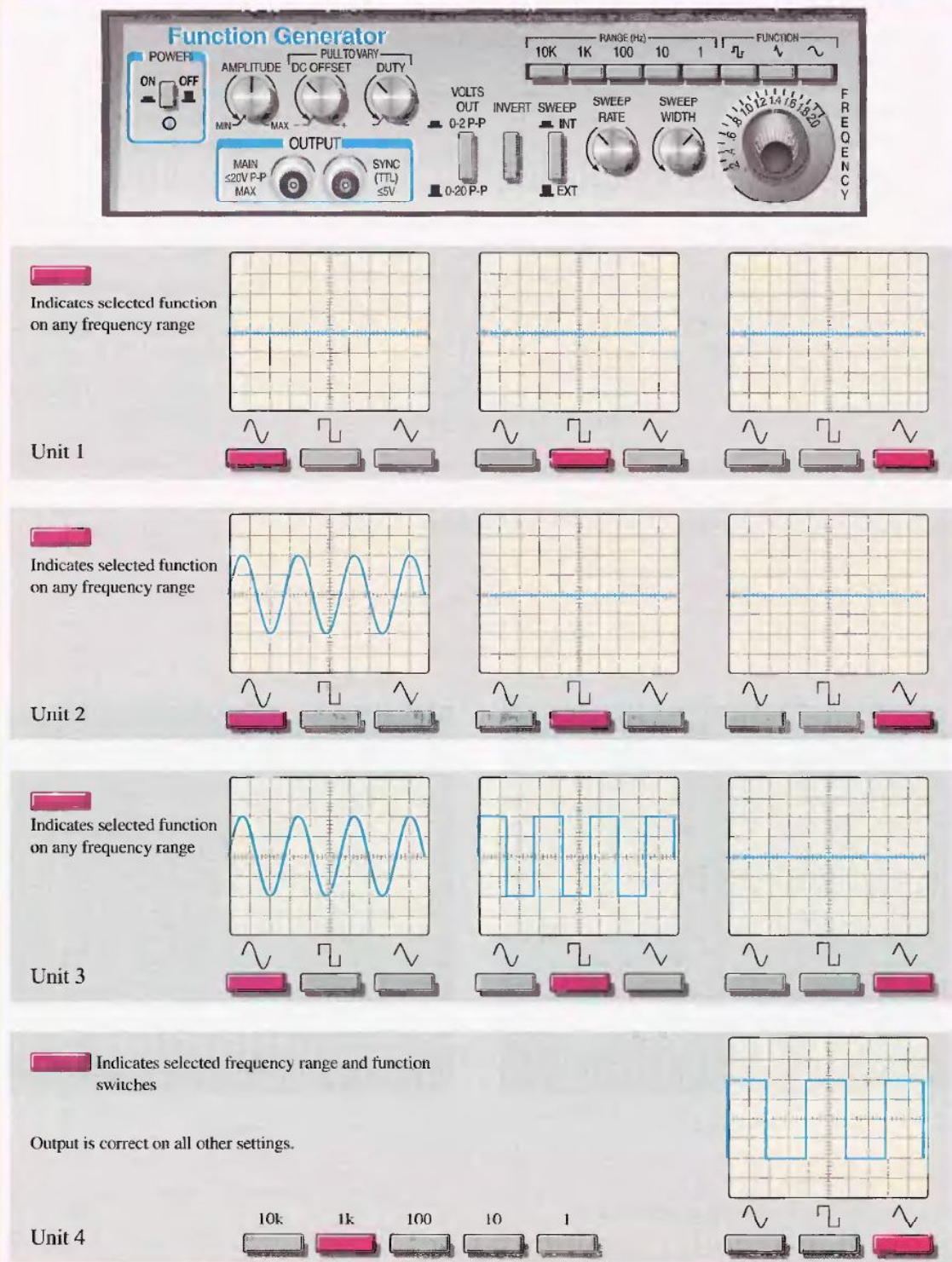


FIGURE 16-48

Results of tests on four faulty units. The scope screen shows the output voltage in each case.

CHAPTER SUMMARY

- Sinusoidal oscillators operate with positive feedback.
- The two conditions for positive feedback are the phase shift around the feedback loop must be 0° and the voltage gain around the feedback loop must equal 1.
- For initial start-up, the voltage gain around the feedback loop must be greater than 1.
- Sinusoidal *RC* oscillators include the Wien-bridge, phase-shift, and twin-T.
- Sinusoidal *LC* oscillators include the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled.
- The feedback signal in a Colpitts oscillator is derived from a capacitive voltage divider in the *LC* circuit.
- The Clapp oscillator is a variation of the Colpitts with a capacitor added in series with the inductor.
- The feedback signal in a Hartley oscillator is derived from an inductive voltage divider in the *LC* circuit.
- The feedback signal in an Armstrong oscillator is derived by transformer coupling.
- Crystal oscillators are the most stable type.
- A relaxation oscillator uses an *RC* timing circuit and a device that changes states to generate a periodic waveform.
- The frequency in a voltage-controlled oscillator (VCO) can be varied with a dc control voltage.
- The 555 timer is an integrated circuit that can be used as an oscillator in addition to many other applications.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Astable Characterized by having no stable states.

Feedback oscillator An electronic circuit that operates with positive feedback and produces a time-varying output signal without an external input signal.

Positive feedback The return of a portion of the output signal to the input such that it reinforces and sustains the output.

Relaxation oscillator An electronic circuit that uses an *RC* timing circuit to generate a nonsinusoidal waveform without an external input signal.

Voltage-controlled oscillator (VCO) A type of relaxation oscillator whose frequency can be varied by a dc control voltage.

KEY FORMULAS

16-1	$\frac{V_{out}}{V_{in}} = \frac{1}{3}$	Wien-bridge positive feedback attenuation
16-2	$f_r = \frac{1}{2\pi RC}$	Wien-bridge resonant frequency
16-3	$B = \frac{1}{29}$	Phase-shift feedback attenuation
16-4	$f_r = \frac{1}{2\pi\sqrt{6RC}}$	Phase-shift oscillator frequency
16-5	$f_r = \frac{1}{2\pi\sqrt{LC_T}}$	Colpitts, Clapp, and Hartley approximate resonant frequency
16-6	$A_v = \frac{C_1}{C_2}$	Colpitts amplifier gain

16-7	$f_r = \frac{1}{2\pi\sqrt{LC_T}} \sqrt{\frac{Q^2}{Q^2 + 1}}$	Colpitts resonant frequency
16-8	$A_v > \frac{L_2}{L_1}$	Hartley self-starting gain
16-9	$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}}$	Armstrong resonant frequency
16-10	$f_r = \frac{1}{4R_1C} \left(\frac{R_2}{R_3} \right)$	Triangular-wave oscillator frequency
16-11	$f = \frac{ V_{IN} }{R_1C} \left(\frac{1}{V_p - V_F} \right)$	Sawtooth VCO frequency
16-12	$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$	555 astable frequency
16-13	Duty cycle = $\left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\%$	555 astable
16-14	Duty cycle = $\left(\frac{R_1}{R_1 + R_2} \right) 100\%$	555 astable (duty cycle < 50%)

CIRCUIT-ACTION QUIZ

Answers are at the end of the chapter.

- If R_1 and R_2 are increased to 18 k Ω in Figure 16-12, the frequency of oscillation will
(a) increase (b) decrease (c) not change
- If the feedback potentiometer R_f is adjusted to a higher value, the voltage gain in Figure 16-12 will
(a) increase (b) decrease (c) not change
- In Figure 16-14, if the R_f is decreased, the feedback attenuation will
(a) increase (b) decrease (c) not change
- If the capacitors in Figure 16-14 are increased to 0.01 μ F, the frequency of oscillation will
(a) increase (b) decrease (c) not change
- In order to increase V_{UTP} in Figure 16-30, R_3 must
(a) increase (b) decrease (c) not change
- If the capacitor in Figure 16-30 opens, the frequency of oscillation will
(a) increase (b) decrease (c) not change
- If the value of R_1 in Figure 16-32 is decreased, the peak value of the sawtooth output will
(a) increase (b) decrease (c) not change
- If the diode in Figure 16-40 opens, the duty cycle will
(a) increase (b) decrease (c) not change

SELF-TEST

Answers are at the end of the chapter.

- An oscillator differs from an amplifier because
(a) it has more gain (b) it requires no input signal
(c) it requires no dc supply (d) it always has the same output
- Wien-bridge oscillators are based on
(a) positive feedback (b) negative feedback
(c) the piezoelectric effect (d) high gain

3. One condition for oscillation is
 - (a) a phase shift around the feedback loop of 180°
 - (b) a gain around the feedback loop of one-third
 - (c) a phase shift around the feedback loop of 0°
 - (d) a gain around the feedback loop of less than 1
4. A second condition for oscillation is
 - (a) no gain around the feedback loop
 - (b) a gain of 1 around the feedback loop
 - (c) the attenuation of the feedback circuit must be one-third
 - (d) the feedback circuit must be capacitive
5. In a certain oscillator, $A_v = 50$. The attenuation of the feedback circuit must be
 - (a) 1 (b) 0.01 (c) 10 (d) 0.02
6. For an oscillator to properly start, the gain around the feedback loop must initially be
 - (a) 1 (b) less than 1 (c) greater than 1 (d) equal to B
7. In a Wien-bridge oscillator, if the resistances in the positive feedback circuit are decreased, the frequency
 - (a) decreases (b) increases (c) remains the same
8. The Wien-bridge oscillator's positive feedback circuit is
 - (a) an RL circuit (b) an LC circuit (c) a voltage divider (d) a lead-lag circuit
9. A phase-shift oscillator has
 - (a) three RC circuits (b) three LC circuits (c) a T-type circuit (d) a π -type circuit
10. Colpitts, Clapp, and Hartley are names that refer to
 - (a) types of RC oscillators (b) inventors of the transistor
 - (c) types of LC oscillators (d) types of filters
11. An oscillator whose frequency is changed by a variable dc voltage is known as
 - (a) a crystal oscillator (b) a VCO
 - (c) an Armstrong oscillator (d) a piezoelectric device
12. The main feature of a crystal oscillator is
 - (a) economy (b) reliability (c) stability (d) high frequency
13. The operation of a relaxation oscillator is based on
 - (a) the charging and discharging of a capacitor
 - (b) a highly selective resonant circuit
 - (c) a very stable supply voltage
 - (d) low power consumption
14. Which one of the following is *not* an input or output of the 555 timer?
 - (a) Threshold (b) Control voltage (c) Clock
 - (d) Trigger (e) Discharge (f) Reset

PROBLEMS

Answers to odd-numbered problems are at the end of the book.

BASIC PROBLEMS

SECTION 16-1 The Oscillator

1. What type of input is required for an oscillator?
2. What are the basic components of an oscillator circuit?

SECTION 16-2 Feedback Oscillator Principles

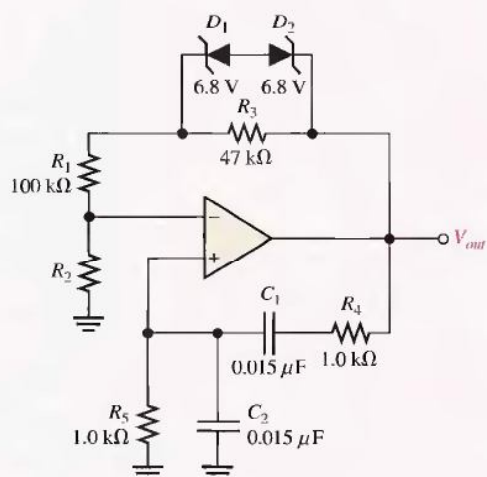
3. If the voltage gain of the amplifier portion of an oscillator is 75, what must be the attenuation of the feedback circuit to sustain the oscillation?

4. Generally describe the change required in the oscillator of Problem 3 in order for oscillation to begin when the power is initially turned on.

SECTION 16-3 Oscillators with RC Feedback Circuits

5. A certain lead-lag circuit has a resonant frequency of 3.5 kHz. What is the rms output voltage if an input signal with a frequency equal to f_r and with an rms value of 2.2 V is applied to the input?
6. Calculate the resonant frequency of a lead-lag circuit with the following values: $R_1 = R_2 = 6.2 \text{ k}\Omega$, and $C_1 = C_2 = 0.02 \text{ }\mu\text{F}$.
7. Determine the necessary value of R_2 in Figure 16-49 so that the circuit will oscillate. Neglect the forward resistance of the zener diodes. (*Hint:* The total gain of the circuit must be 3 when the zener diodes are conducting.)
8. Explain the purpose of R_3 in Figure 16-49.

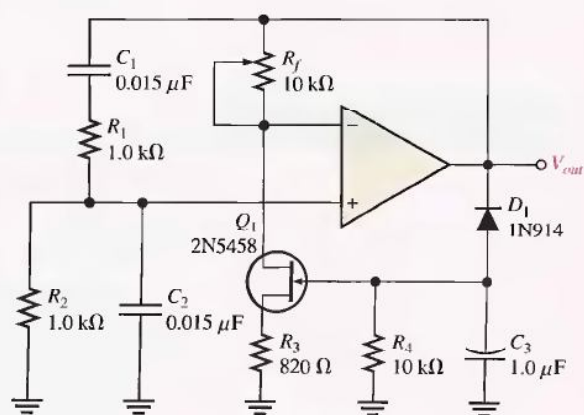
FIGURE 16-49



9. For the Wien-bridge oscillator in Figure 16-50, calculate the setting for R_f , assuming the internal drain-source resistance, r'_{ds} , of the JFET is $350 \text{ }\Omega$ when oscillations are stable.
10. Find the frequency of oscillation for the Wien-bridge oscillator in Figure 16-50.

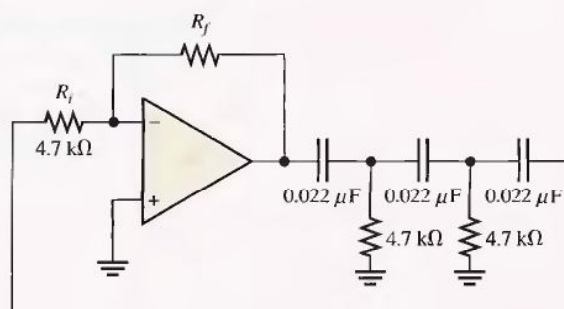
FIGURE 16-50

Multisim file circuits are identified with a CD logo and are in the Problems folder on your CD-ROM. Filenames correspond to figure numbers (e.g., F16-50).





► FIGURE 16-51

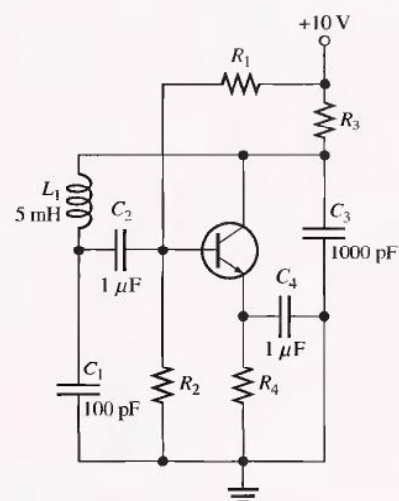


11. What value of R_f is required in Figure 16-51? What is f_r ?

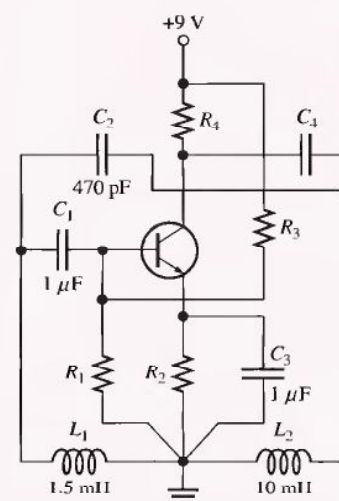
SECTION 16-4 Oscillators with LC Feedback Circuits

12. Calculate the frequency of oscillation for each circuit in Figure 16-52 and identify the type of oscillator. Assume $Q > 10$ in each case.

► FIGURE 16-52



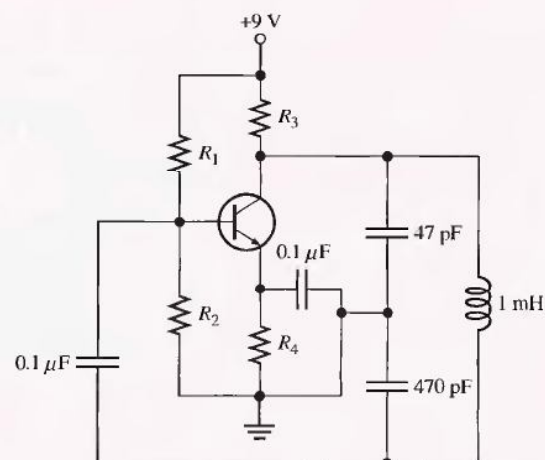
(a)



(b)

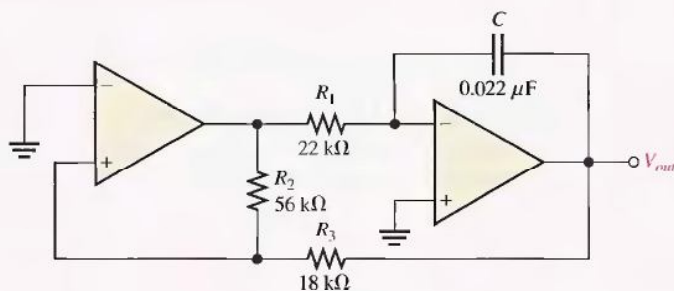
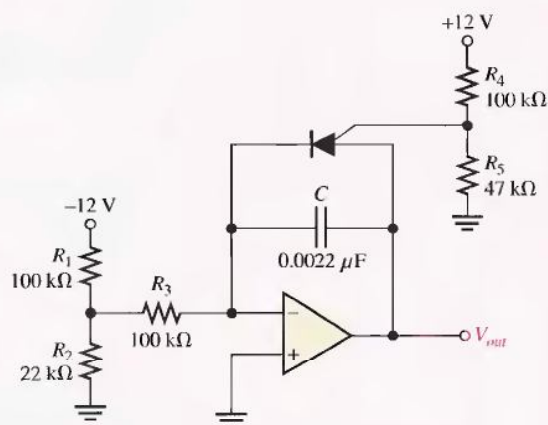
13. Determine what the gain of the amplifier stage must be in Figure 16-53 in order to have sustained oscillation.

► FIGURE 16-53



SECTION 16-5 Relaxation Oscillators

14. What type of signal does the circuit in Figure 16-54 produce? Determine the frequency of the output.
15. Show how to change the frequency of oscillation in Figure 16-54 to 10 kHz.
16. Determine the amplitude and frequency of the output voltage in Figure 16-55. Use 1 V as the forward PUT voltage.

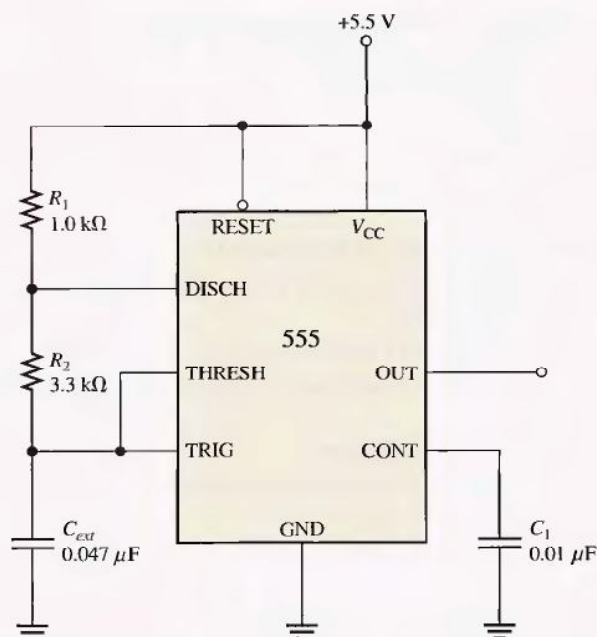
FIGURE 16-54**FIGURE 16-55**

17. Modify the sawtooth generator in Figure 16-55 so that its peak-to-peak output is 4 V.
18. A certain sawtooth generator has the following parameter values: $V_{IN} = 3 \text{ V}$, $R = 4.7 \text{ k}\Omega$, $C = 0.001 \text{ }\mu\text{F}$. Determine its peak-to-peak output voltage if the period is $10 \text{ }\mu\text{s}$.

SECTION 16-6 The 555 Timer as an Oscillator

19. What are the two comparator reference voltages in a 555 timer when $V_{CC} = 10 \text{ V}$?
20. Determine the frequency of oscillation for the 555 astable oscillator in Figure 16-56.
21. To what value must C_{ext} be changed in Figure 16-56 to achieve a frequency of 25 kHz?
22. In an astable 555 configuration, the external resistor $R_1 = 3.3 \text{ k}\Omega$. What must R_2 equal to produce a duty cycle of 75 percent?

FIGURE 16-56



MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on your CD-ROM.

23. Open file TSP16-23 and determine the fault.
24. Open file TSP16-24 and determine the fault.
25. Open file TSP16-25 and determine the fault.
26. Open file TSP16-26 and determine the fault.
27. Open file TSP16-27 and determine the fault.
28. Open file TSP16-28 and determine the fault.

ANSWERS

SECTION REVIEWS

SECTION 16-1 The Oscillator

1. An oscillator is a circuit that produces a repetitive output waveform with only the dc supply voltage as an input.
2. Positive feedback
3. The feedback circuit provides attenuation and phase shift.
4. Feedback and relaxation

SECTION 16-2 Feedback Oscillator Principles

1. Zero phase shift and unity voltage gain around the closed feedback
2. Positive feedback is when a portion of the output signal is fed back to the input of the amplifier such that it reinforces itself.
3. Loop gain greater than 1

SECTION 16-3 Oscillators with RC Feedback Circuits

1. The negative feedback loop sets the closed-loop gain; the positive feedback loop sets the frequency of oscillation.
2. 1.67 V
3. The three RC circuits contribute a total of 180° , and the inverting amplifier contributes 180° for a total of 360° around the loop.

SECTION 16-4 Oscillators with LC Feedback Circuits

1. Colpitts uses a capacitive voltage divider in the feedback circuit; Hartley uses an inductive voltage divider.
2. The higher FET input impedance has less loading effect on the resonant feedback circuit.
3. A Clapp has an additional capacitor in series with the inductor in the feedback circuit.

SECTION 16-5 Relaxation Oscillators

1. A voltage-controlled oscillator exhibits a frequency that can be varied with a dc control voltage.
2. The basis of a relaxation oscillator is the charging and discharging of a capacitor.

SECTION 16-6 The 555 Timer as an Oscillator

1. Two comparators, a flip-flop, a discharge transistor, and a resistive voltage divider
2. The duty cycle is set by the external resistors.

RELATED PROBLEMS FOR EXAMPLES

16-1 Instability may occur in either case.

16-2 (a) 238 k Ω (b) 7.92 kHz

16-3 7.24 kHz

16-4 6.06 V peak-to-peak

16-5 1122 Hz

16-6 31.9%

CIRCUIT-ACTION QUIZ

1. (b) 2. (a) 3. (a) 4. (b) 5. (a) 6. (b) 7. (c) 8. (a)

SELF-TEST

1. (b) 2. (a) 3. (c) 4. (b) 5. (d) 6. (c) 7. (b)
 8. (d) 9. (a) 10. (c) 11. (b) 12. (c) 13. (a) 14. (c)

17

COMMUNICATIONS CIRCUITS

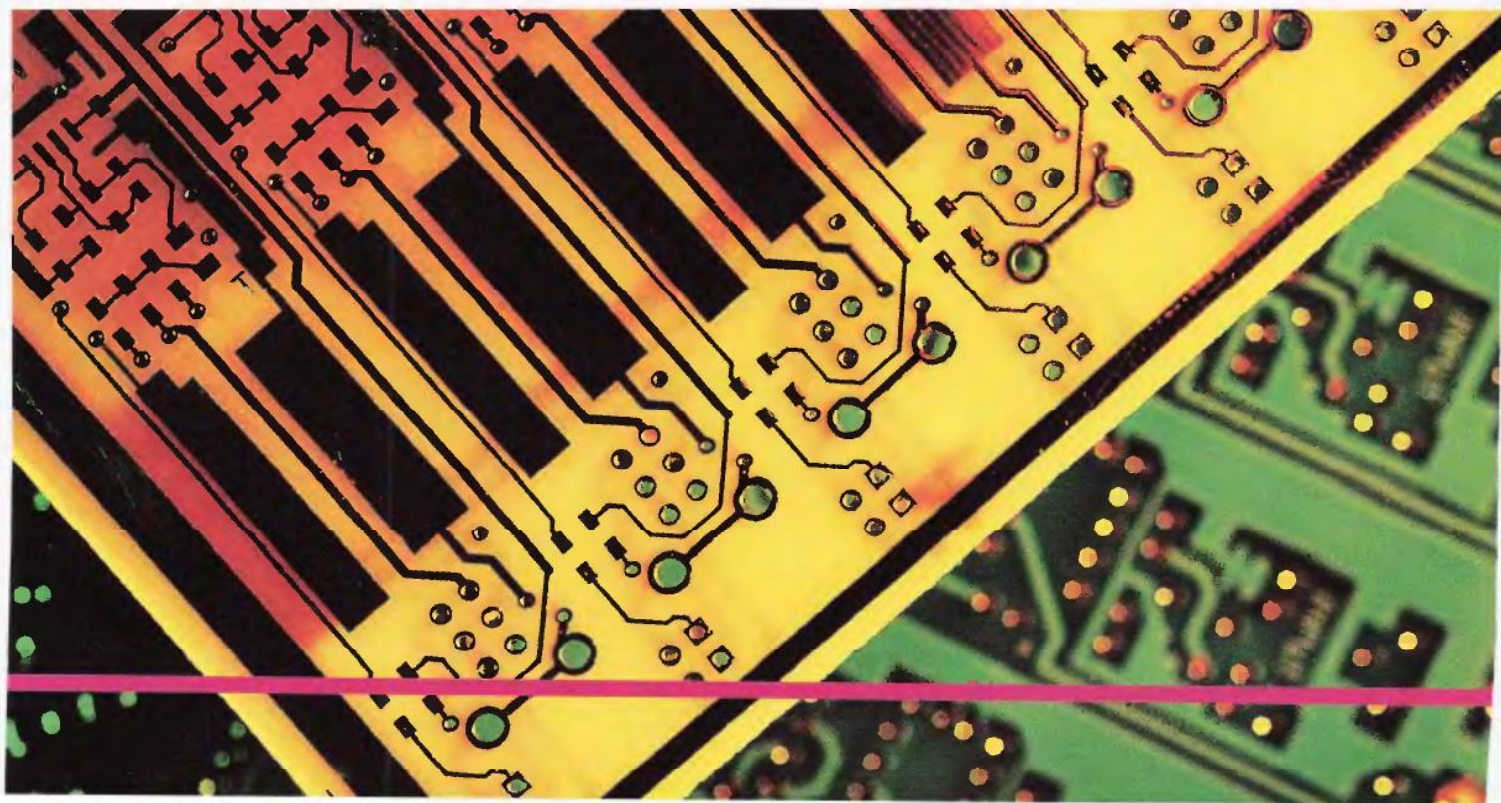
INTRODUCTION

Communications electronics encompasses a wide range of systems, including both analog and digital. Any system that sends information from one point to another over relatively long distances can be classified as a communications system. Some of the categories of communications systems are radio (broadcast, ham, CB, marine), television, telephony, radar, navigation, satellite, data (digital), and telemetry.

Many communications systems use either amplitude modulation (AM) or frequency modulation (FM) to send information. Other modulation methods include pulse modulation, phase modulation, and frequency shift keying (FSK) as well as more specialized techniques. By necessity, the scope of this chapter is limited and is intended to introduce you to basic AM and FM communications systems and circuits.

CHAPTER OUTLINE

- 17-1 Basic Receivers
- 17-2 The Linear Multiplier
- 17-3 Amplitude Modulation
- 17-4 The Mixer
- 17-5 AM Demodulation
- 17-6 IF and Audio Amplifiers
- 17-7 Frequency Modulation
- 17-8 The Phase-Locked Loop (PLL)
-  System Application



CHAPTER OBJECTIVES

- Describe basic superheterodyne receivers
- Discuss the function of a linear multiplier
- Discuss the fundamentals of amplitude modulation
- Discuss the basic function of a mixer
- Describe AM demodulation
- Describe IF and audio amplifiers
- Describe frequency modulation
- Describe a phase-locked loop (PLL)

KEY TERMS

- Amplitude modulation (AM)
- Frequency modulation (FM)
- Four-quadrant multiplier
- Balanced modulation
- Mixer
- Phase-locked loop (PLL)
- Lock range
- Capture range

SYSTEM APPLICATION PREVIEW

Digital data consisting of a series of binary digits (1s and 0s) are commonly sent from one computer to another over the telephone lines. Two voltage levels are used to represent the two types of bits, a high-voltage level and a low-voltage level. The data stream is made up of time intervals when the voltage has a constant high value or a constant low value with very fast transitions from one level to the other. In other words, the data stream contains very low frequencies (constant-voltage intervals) and very high frequencies (transitions). Since the standard telephone system has a bandwidth of approximately 300 Hz to 3000 Hz, it cannot handle the very low and the very high frequencies that make up a typical data stream without losing most of the information. Because of the bandwidth limitation of the telephone system, it is necessary to modify digital data before they are sent out; and one method of doing this is with frequency shift keying (FSK), which is a form of frequency modulation.

A simplified block diagram of a digital communications equipment (DCE) system for interfacing digital terminal equipment (DTE), such as a computer, to the telephone network is shown in the system application. The system FSK-modulates digital data before they are transmitted over the phone line and demodulates FSK signals received from another computer. Because the DCE's basic function is to *modulate* and *demodulate*, it is called a **modem**. Although the modem performs many associated functions, in this system application our focus will be on the modulation and demodulation circuits.

WWW. VISIT THE COMPANION WEBSITE

Study aids for this chapter are available at
<http://www.prenhall.com/floyd>

17-1 BASIC RECEIVERS

Receivers based on the superheterodyne principle are standard in one form or another in most types of communications systems and are found in familiar systems such as standard broadcast radio, stereo, and television. In several of the system applications in previous chapters, we presented the superheterodyne receiver in order to focus on a given circuit; now we cover it from a system viewpoint. This section provides a basic introduction to amplitude modulation and frequency modulation and an overview of the complete AM and FM receiver.

After completing this section, you should be able to

- Describe basic superheterodyne receivers
- Define *AM* and *FM*
- Discuss the major functional blocks of an AM receiver
- Discuss the major functional blocks of an FM receiver

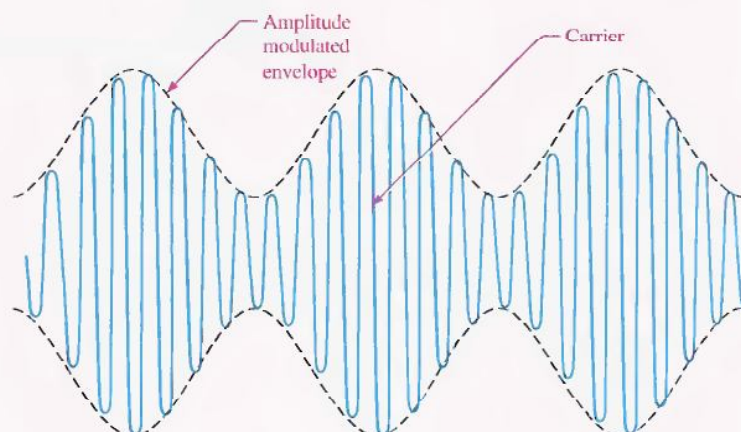
Amplitude Modulation



Amplitude modulation (AM) is a method for sending audible information, such as voice and music, by electromagnetic waves that are broadcast through the atmosphere. In AM, the amplitude of a signal with a specific frequency (f_c), called the *carrier*, is varied according to a modulating signal, which can be an audio signal (voice or music), as shown in Figure 17-1. The carrier frequency permits the receiver to be tuned to a specific known frequency. The resulting AM waveform contains the carrier frequency, an upper-side frequency equal to the carrier frequency plus the modulation frequency ($f_c + f_m$), and a lower-side frequency equal to the carrier frequency minus the modulation frequency ($f_c - f_m$). For example, if a 1 MHz carrier is amplitude modulated with a 5 kHz audio signal, the frequency components in the AM waveform are 1 MHz (carrier), 1 MHz + 5 kHz = 1,005,000 Hz (upper side), and 1 MHz - 5 kHz = 995,000 Hz (lower side). Harmonics of these frequencies are also present.

► **FIGURE 17-1**

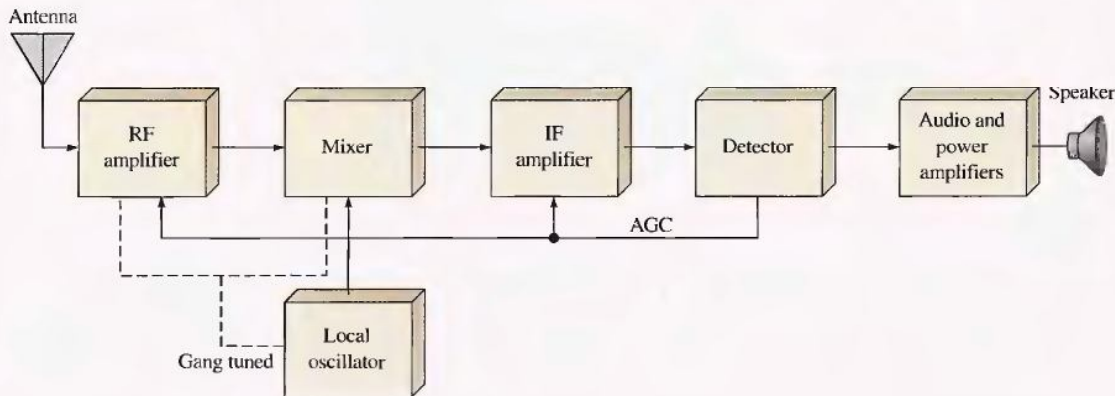
An example of an amplitude modulated signal. In this case, the higher-frequency carrier is modulated by a lower-frequency sinusoidal signal.



The frequency band for AM broadcast receivers is 540 kHz to 1640 kHz. This means that an AM receiver can be tuned to pick up a specific carrier frequency that lies in the broadcast band. Each AM radio station transmits at a specific carrier frequency that is different from any other station in the area, so you can tune the receiver to pick up any desired station.

The Superheterodyne AM Receiver

A block diagram of a superheterodyne AM receiver is shown in Figure 17-2. The receiver shown consists of an antenna, an RF (radio frequency) amplifier, a mixer, a local oscillator (LO), an IF (intermediate frequency) amplifier, a detector, an audio amplifier, a power amplifier, and a speaker.



▲ FIGURE 17-2

Superheterodyne AM receiver block diagram.

Antenna The antenna picks up all radiated signals and feeds them into the RF amplifier. These signals are very small (usually only a few microvolts).

RF Amplifier This circuit can be adjusted (tuned) to select and amplify any carrier frequency within the AM broadcast band. Only the selected frequency and its two side bands pass through the amplifier. (Some AM receivers do not have a separate RF amplifier stage.)

Local Oscillator This circuit generates a steady sine wave at a frequency 455 kHz above the selected RF frequency.

Mixer This circuit accepts two inputs, the amplitude modulated RF signal from the output of the RF amplifier (or the antenna when there is no RF amplifier) and the sinusoidal output of the local oscillator (LO). These two signals are then “mixed” by a nonlinear process called *heterodyning* to produce sum and difference frequencies. For example, if the RF carrier has a frequency of 1000 kHz, the LO frequency is 1455 kHz and the sum and difference frequencies out of the mixer are 2455 kHz and 455 kHz, respectively. The difference frequency is always 455 kHz no matter what the RF carrier frequency.

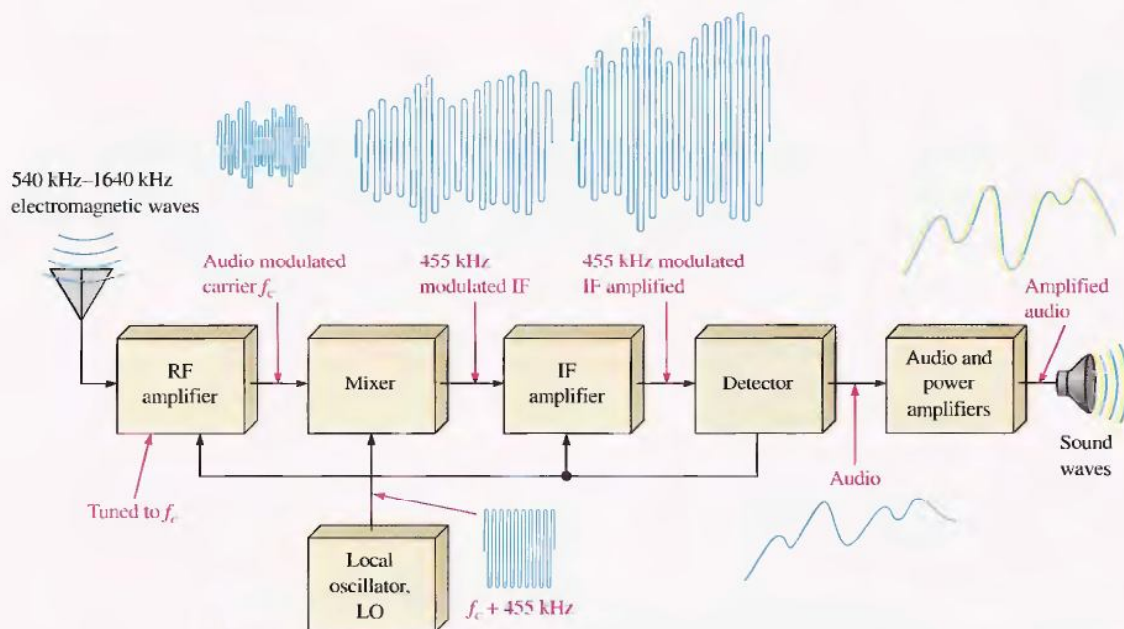
IF Amplifier The input to the IF amplifier is the 455 kHz AM signal, a replica of the original AM carrier signal except that the frequency has been lowered to 455 kHz. The IF amplifier significantly increases the level of this signal.

Detector This circuit recovers the modulating signal (audio signal) from the 455 kHz intermediate frequency (IF). At this point the IF is no longer needed, so the output of the detector consists of only the audio signal.

Audio and Power Amplifiers This circuit amplifies the detected audio signal and drives the speaker to produce sound.

AGC The automatic gain control (AGC) provides a dc level out of the detector that is proportional to the strength of the received signal. This level is fed back to the IF amplifier, and sometimes to the mixer and RF amplifier, to adjust the gains so as to maintain constant signal levels throughout the system over a wide range of incoming carrier signal strengths.

Figure 17-3 shows the signal flow through an AM superheterodyne receiver. The receiver can be tuned to accept any frequency in the AM band. The RF amplifier, mixer, and local oscillator are tuned simultaneously so that the LO frequency is always 455 kHz above the incoming RF signal frequency. This is called *gang tuning*.



▲ FIGURE 17-3

Illustration of signal flow through an AM receiver.

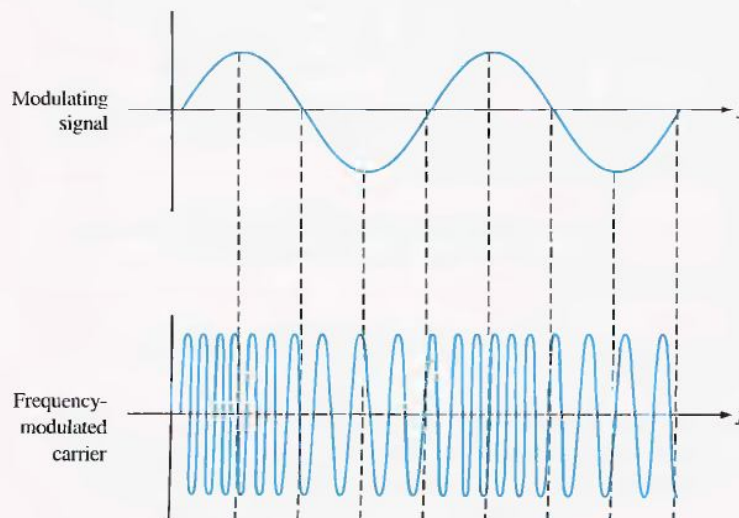
Frequency Modulation



In **frequency modulation (FM)**, the modulating signal (audio) varies the frequency of a carrier as opposed to the amplitude, as in the case of AM. Figure 17-4 illustrates basic frequency modulation. The standard FM broadcast band consists of carrier frequencies from 88 MHz to 108 MHz, which is significantly higher than AM.

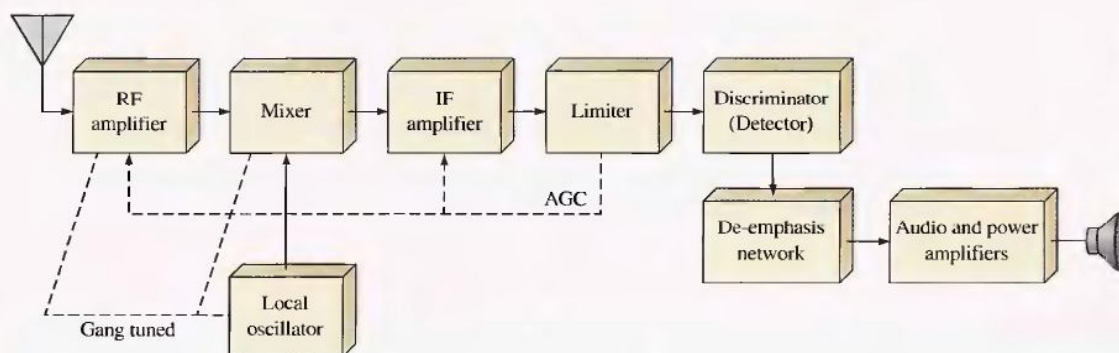
► FIGURE 17-4

An example of frequency modulation.



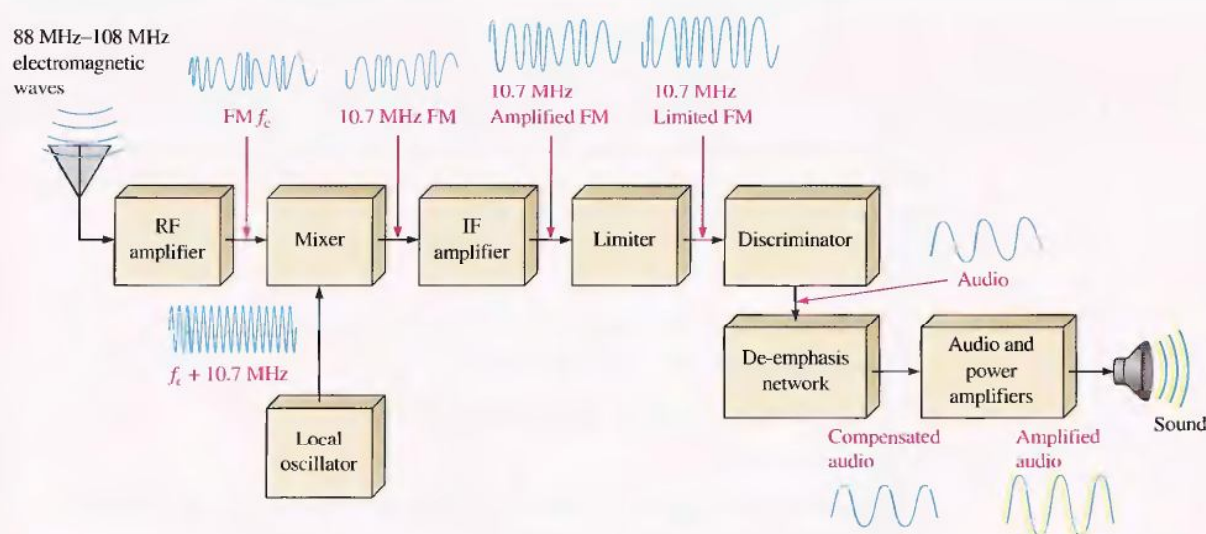
The Superheterodyne FM Receiver

The FM receiver is similar to the AM receiver in many ways, but there are several differences. A block diagram of a superheterodyne FM receiver is shown in Figure 17-5. Notice that it includes an RF amplifier, mixer, local oscillator, and IF amplifier just as in the AM receiver. These circuits must, however, operate at higher frequencies than in the AM system. A significant difference in FM is the way the audio signal must be recovered from the modulated IF. This is accomplished by the limiter, discriminator, and de-emphasis network. Figure 17-6 depicts the signal flow through an FM receiver.



▲ FIGURE 17-5

Superheterodyne FM receiver block diagram.



▲ FIGURE 17-6

Example of signal flow through an FM receiver.

RF Amplifier This circuit must be capable of amplifying any frequency between 88 MHz and 108 MHz. It is highly selective so that it passes only the selected carrier frequency and significant side-band frequencies that contain the audio.

Local Oscillator This circuit produces a sine wave at a frequency 10.7 MHz above the selected RF frequency.

Mixer This circuit performs the same function as in the AM receiver, except that its output is a 10.7 MHz FM signal regardless of the RF carrier frequency.

IF Amplifier This circuit amplifies the 10.7 MHz FM signal.

Limiter The limiter removes any unwanted variations in the amplitude of the FM signal as it comes out of the IF amplifier and produces a constant amplitude FM output at the 10.7 MHz intermediate frequency.

Discriminator This circuit performs the equivalent function of the detector in an AM system and is sometimes called a detector rather than a discriminator. The **discriminator** recovers the audio from the FM signal.

De-emphasis Network For certain reasons, the higher modulating frequencies are amplified more than the lower frequencies at the transmitting end of an FM system by a process called *preemphasis*. The de-emphasis circuit in the FM receiver brings the high-frequency audio signals back to the proper amplitude relationship with the lower frequencies.

Audio and Power Amplifiers This circuit is the same as in the AM system and can be shared when there is a dual AM/FM configuration.

SECTION 17-1 REVIEW

Answers are at the end of the chapter.

1. What do *AM* and *FM* mean?
2. How do *AM* and *FM* differ?
3. What are the standard broadcast frequency bands for *AM* and *FM*?

17-2 THE LINEAR MULTIPLIER

The linear multiplier is a key circuit in many types of communications systems. In this section, you will examine the basic principles of IC linear multipliers and look at a few applications that are found in communications as well as in other areas. In the following sections, we will concentrate on multiplier applications in AM and FM systems.

After completing this section, you should be able to

- Discuss the function of a linear multiplier
- Describe multiplier quadrants and transfer characteristic
- Discuss scale factor
- Show how to use a multiplier circuit as a multiplier, squaring circuit, divide circuit, square root circuit, and mean square circuit

Multiplier Quadrants

There are one-quadrant, two-quadrant, and four-quadrant multipliers. The quadrant classification indicates the number of input polarity combinations that the multiplier can handle. A graphical representation of the quadrants is shown in Figure 17-7. A **four-quadrant multiplier** can accept any of the four possible input polarity combinations and produce an output with the corresponding polarity.



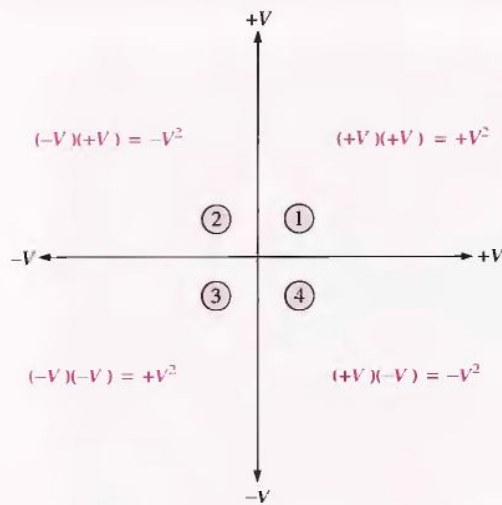


FIGURE 17-7

Four-quadrant polarities and their products.

The Multiplier Transfer Characteristic

Figure 17-8 shows the transfer characteristic for a typical IC linear multiplier of two input voltages V_X and V_Y . Values of V_X run along the horizontal axis and values of V_Y are the sloped lines. To find the output voltage from the transfer characteristic graph, find the intersection of the two input voltages V_X and V_Y . Then find the output voltage by projecting the point of intersection over to the vertical axis. An example will illustrate this.

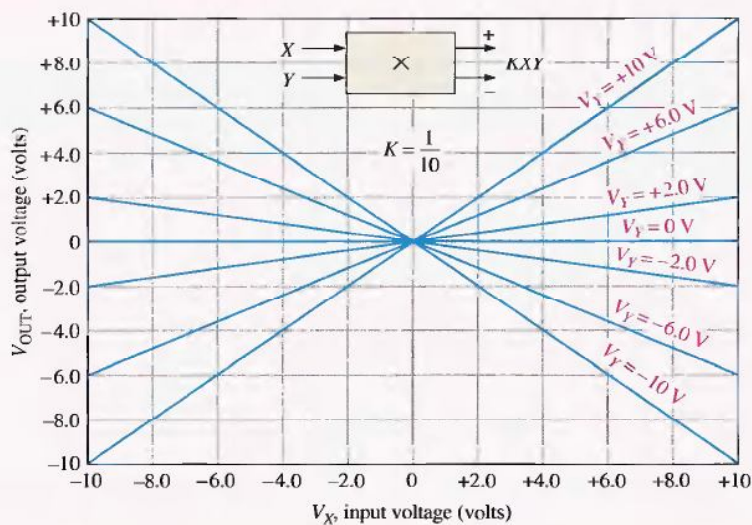


FIGURE 17-8

A four-quadrant multiplier transfer characteristic.

EXAMPLE 17-1

Determine the output voltage for a four-quadrant linear multiplier whose transfer characteristic is given in Figure 17-8. The input voltages are $V_X = -4\text{ V}$ and $V_Y = +10\text{ V}$.

Solution The output voltage is -4 V as illustrated in Figure 17-9. For this transfer characteristic, the output voltage is a factor of ten smaller than the actual product of the two input voltages. This is due to the scale factor of the multiplier, which is discussed next.

The current I_{R2} is set by internal and external parameters according to this formula:

$$I_{R2} = \frac{|-V| - 0.7 \text{ V}}{R_2 + 500 \Omega}$$

where R_2 is the combination of the fixed resistor and the potentiometer. The potentiometer provides for fine adjustment by controlling I_{R2} .

The expression for the output voltage of the IC linear multiplier includes the scale factor, K , as indicated in Equation 17-1.

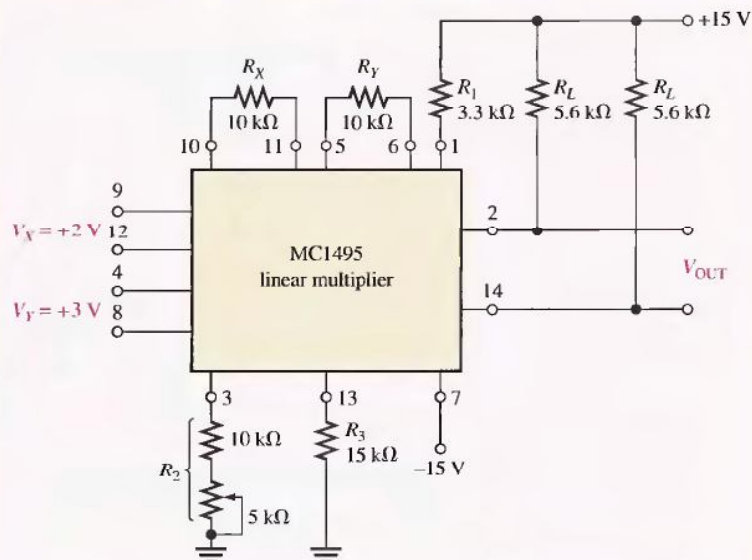
$$V_{\text{OUT}} = KV_XV_Y$$

Equation 17-1

EXAMPLE 17-2

Determine the scale factor for the basic MC1495 multiplier in Figure 17-11. Assume the 5 k Ω potentiometer portion of R_2 is set to 2.5 k Ω . Also, determine the output voltage for the given inputs.

FIGURE 17-11



Solution Calculate I_{R2} .

$$I_{R2} = \frac{|-V| - 0.7 \text{ V}}{R_2 + 500 \Omega} = \frac{15 \text{ V} - 0.7 \text{ V}}{12.5 \text{ k}\Omega + 500 \Omega} = \frac{14.3 \text{ V}}{13 \text{ k}\Omega} = 1.1 \text{ mA}$$

The scale factor is

$$K = \frac{2R_L}{R_X R_Y I_{R2}} = \frac{2(5.6 \text{ k}\Omega)}{(10 \text{ k}\Omega)(10 \text{ k}\Omega)(1.1 \text{ mA})} = 0.102$$

The output voltage is

$$V_{\text{OUT}} = KV_XV_Y = 0.102 (+2 \text{ V})(+3 \text{ V}) = 0.611 \text{ V}$$

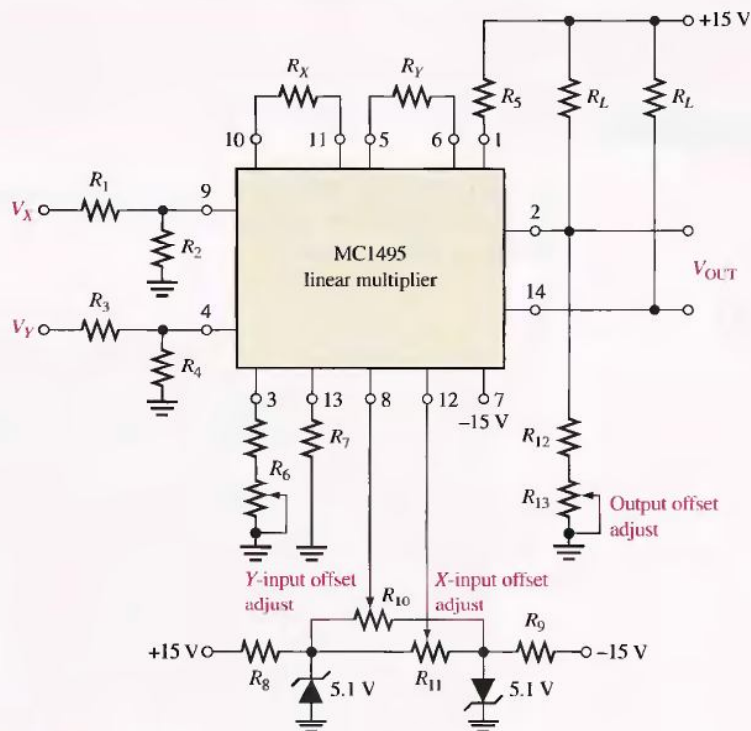
Related Problem What is the output voltage in Figure 17-11 if the 5 k Ω potentiometer is set to its maximum resistance?

Offset Adjustment

Due to internal mismatches, small offset voltages are usually at the inputs and the output of an IC linear multiplier. External circuits to null out the offset voltages are shown in Figure 17-12. The resistive voltage dividers on the inputs allow the actual input voltages to be greater than the recommended maximum for the device. For example, the MC1495 has a maximum input voltage of 5 V. The voltage dividers allow a maximum of 10 V to be applied if the resistors are of equal value. The zener diodes in the input offset adjust circuit keep the inputs on pins 8 and 12 from exceeding the maximum of 5 V.

► **FIGURE 17-12**

Basic MC1495 multiplier with both scale factor and offset circuitry.



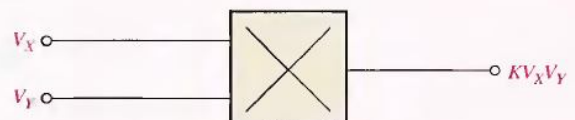
Basic Applications of the Multiplier

Applications of linear multipliers are numerous. Some basic applications are now presented.

Multiplier The most obvious application of a linear multiplier is, of course, to multiply two voltages as indicated in Figure 17-13.

► **FIGURE 17-13**

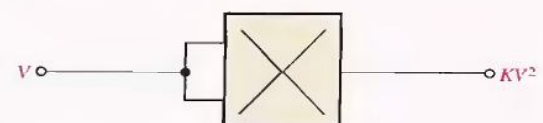
Multiplier.



Squaring Circuit A special case of the multiplier is a squaring circuit that is realized by simply applying the same voltage to both inputs by connecting the inputs together as shown in Figure 17-14.

► **FIGURE 17-14**

Squaring circuit.



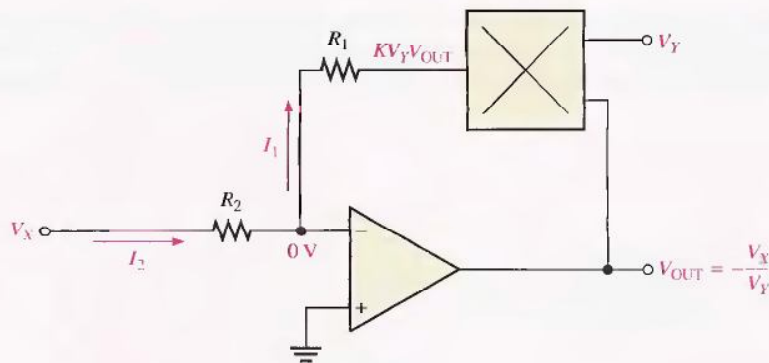


FIGURE 17-15

Divide circuit.

Divide Circuit The circuit in Figure 17-15 shows the multiplier placed in the feedback loop of an op-amp. The basic operation is as follows. There is a virtual ground at the inverting (−) input of the op-amp and therefore the current at the inverting input is negligible. Therefore, I_1 and I_2 are equal. Since the inverting input voltage is 0 V, the voltage across R_1 is KV_YV_{OUT} and the current through R_1 is

$$I_1 = \frac{KV_YV_{OUT}}{R_1}$$

The voltage across R_2 is V_X , so the current through R_2 is

$$I_2 = \frac{V_X}{R_2}$$

Since $I_1 = -I_2$,

$$\frac{KV_YV_{OUT}}{R_1} = -\frac{V_X}{R_2}$$

Solving for V_{OUT} ,

$$V_{OUT} = -\frac{V_X R_1}{KV_Y R_2}$$

If $R_1 = KR_2$,

$$V_{OUT} = -\frac{V_X}{V_Y}$$

Square Root Circuit The square root circuit is a special case of the divide circuit where V_{OUT} is applied to both inputs of the multiplier as shown in Figure 17-16.

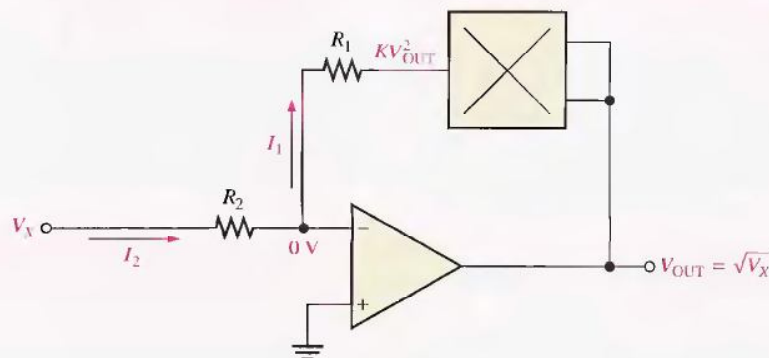


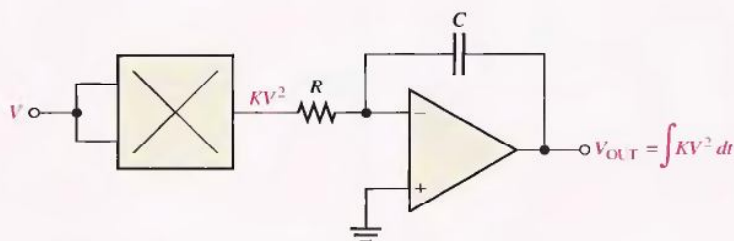
FIGURE 17-16

Square root circuit.

Mean Square Circuit In this application, the multiplier is used as a squaring circuit with its output connected to an op-amp integrator as shown in Figure 17-17. The integrator produces the average or mean value of the squared input over time, as indicated by the integration sign ($\int$).

FIGURE 17-17

Mean square circuit.



SECTION 17-2 REVIEW

1. Compare a four-quadrant multiplier to a one-quadrant multiplier in terms of the inputs that can be handled.
2. If 5 V and 1 V are applied to the inputs of a multiplier and its output is 0.5 V, what is the scale factor? What must the scale factor be for an output of 5 V?
3. How do you convert a basic multiplier to a squaring circuit?

17-3 AMPLITUDE MODULATION

Amplitude modulation (AM) is an important method for transmitting information. Of course, the AM superheterodyne receiver is designed to receive transmitted AM signals. In this section, we take a further look at amplitude modulation and show how the linear multiplier can be used as an amplitude-modulated device.

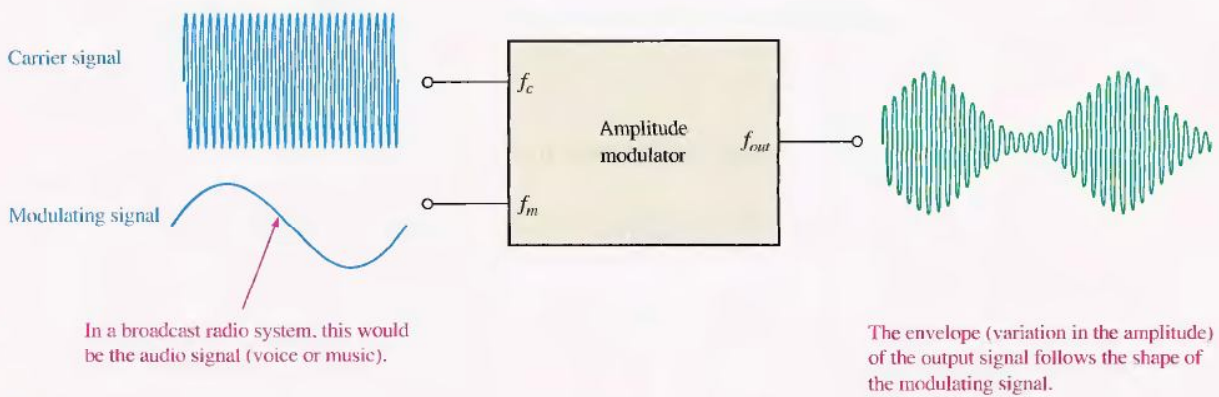
After completing this section, you should be able to

- Discuss the fundamentals of amplitude modulation
- Explain how AM is basically a multiplication process
- Describe sum and difference frequencies
- Discuss balanced modulation
- Describe the frequency spectra
- Explain standard AM

As you learned in Section 17-1, amplitude modulation is the process of varying the amplitude of a signal of a given frequency (carrier) with another signal of much lower frequency (modulating signal). One reason that the higher-frequency carrier signal is necessary is because audio or other signals with relatively low frequencies cannot be transmitted with antennas of a practical size. The basic concept of standard amplitude modulation is illustrated in Figure 17-18.

A Multiplication Process

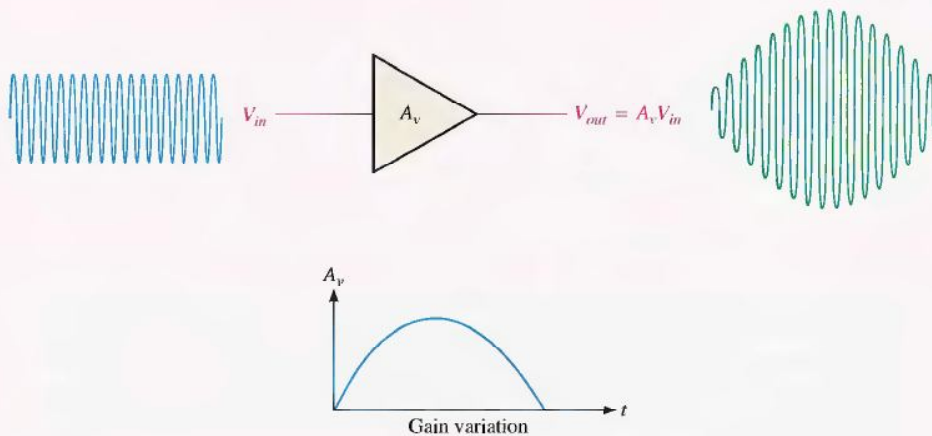
If a signal is applied to the input of a variable-gain device, the resulting output is an amplitude-modulated signal because $V_{out} = A_v V_{in}$. The output voltage is the input voltage



▲ **FIGURE 17-18**

Basic concept of amplitude modulation.

multiplied by the voltage gain. For example, if the gain of an amplifier is made to vary sinusoidally at a certain frequency and an input signal is applied at a higher frequency, the output signal will have the higher frequency. However, its amplitude will vary according to the variation in gain as illustrated in Figure 17-19. Amplitude modulation is basically a multiplication process (input voltage multiplied by a variable gain).



▲ **FIGURE 17-19**

The amplitude of the output voltage varies according to the gain and is the product of voltage gain and input voltage.

Sum and Difference Frequencies

If the expressions for two sinusoidal signals of different frequencies are multiplied mathematically, a term containing both the difference and the sum of the two frequencies is produced. Recall from ac circuit theory that a sinusoidal voltage can be expressed as

$$v = V_p \sin 2\pi ft$$

where V_p is the peak voltage and f is the frequency. Two different sinusoidal signals can be expressed as follows:

$$v_1 = V_{1(p)} \sin 2\pi f_1 t$$

$$v_2 = V_{2(p)} \sin 2\pi f_2 t$$

Multiplying these two sinusoidal wave terms,

$$v_1 v_2 = (V_{1(p)} \sin 2\pi f_1 t)(V_{2(p)} \sin 2\pi f_2 t) = V_{1(p)} V_{2(p)} (\sin 2\pi f_1 t)(\sin 2\pi f_2 t)$$

The general trigonometric identity for the product of two sinusoidal functions is

$$(\sin A)(\sin B) = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$$

Applying this identity to the previous formula for v_1v_2 ,

$$\begin{aligned} v_1v_2 &= \frac{V_{1(p)}V_{2(p)}}{2}[\cos(2\pi f_1t - 2\pi f_2t) - \cos(2\pi f_1t + 2\pi f_2t)] \\ &= \frac{V_{1(p)}V_{2(p)}}{2}[\cos 2\pi(f_1 - f_2)t - \cos 2\pi(f_1 + f_2)t] \end{aligned}$$

Equation 17-2

$$v_1v_2 = \frac{V_{1(p)}V_{2(p)}}{2}\cos 2\pi(f_1 - f_2)t - \frac{V_{1(p)}V_{2(p)}}{2}\cos 2\pi(f_1 + f_2)t$$

You can see in Equation 17-2 that the product of the two sinusoidal voltages V_1 and V_2 contains a difference frequency ($f_1 - f_2$) and a sum frequency ($f_1 + f_2$). The fact that the product terms are cosine simply indicates a 90° phase shift in the multiplication process.

Analysis of Balanced Modulation

Since amplitude modulation is simply a multiplication process, the preceding analysis is now applied to carrier and modulating signals. The expression for the sinusoidal carrier signal can be written as

$$v_c = V_{c(p)}\sin 2\pi f_c t$$

Assuming a sinusoidal modulating signal, it can be expressed as

$$v_m = V_{m(p)}\sin 2\pi f_m t$$

Substituting these two signals in Equation 17-2,

$$v_cv_m = \frac{V_{c(p)}V_{m(p)}}{2}\cos 2\pi(f_c - f_m)t - \frac{V_{c(p)}V_{m(p)}}{2}\cos 2\pi(f_c + f_m)t$$

An output signal described by this expression for the product of two sinusoidal signals is produced by a linear multiplier. Notice that there is a difference frequency term ($f_c - f_m$) and a sum frequency term ($f_c + f_m$), but the original frequencies, f_c and f_m , do not appear alone in the expression. Thus, the product of two sinusoidal signals contains no signal with the carrier frequency, f_c , or with the modulating frequency, f_m . This form of amplitude modulation is called **balanced modulation** because there is no carrier frequency in the output. The carrier frequency is “balanced out.”

The Frequency Spectra of a Balanced Modulator

A graphical picture of the frequency content of a signal is called its frequency spectrum. A frequency spectrum shows voltage on a frequency base rather than on a time base as a waveform diagram does. The frequency spectra of the product of two sinusoidal signals are shown in Figure 17-20. Part (a) shows the two input frequencies and part (b) shows the output frequencies. In communications terminology, the sum frequency is called the **upper-side frequency** and the difference frequency is called the **lower-side frequency** because the frequencies appear on each side of the missing carrier frequency.

The Linear Multiplier as a Balanced Modulator

As mentioned, the linear multiplier acts as a balanced modulator when a carrier signal and a modulating signal are applied to its inputs, as illustrated in Figure 17-21. A balanced modulator produces an upper-side frequency and a lower-side frequency, but it does not

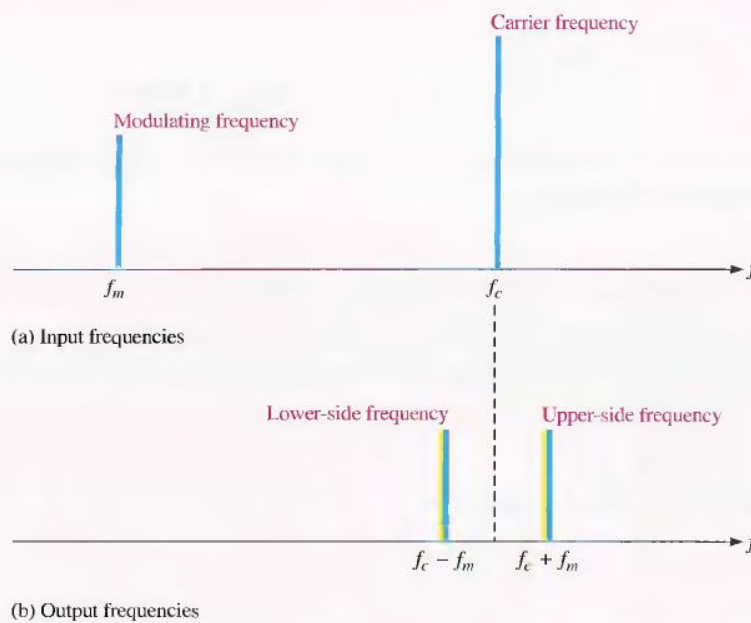


FIGURE 17-20

Illustration of the input and output frequency spectra for a linear multiplier.

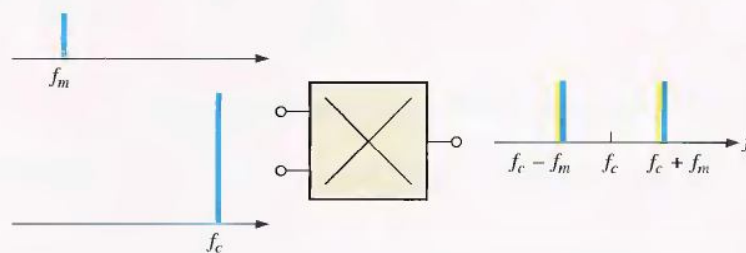


FIGURE 17-21

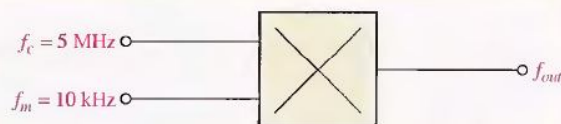
The linear multiplier as a balanced modulator.

produce a carrier frequency. Since there is no carrier signal, balanced modulation is sometimes known as **suppressed-carrier modulation**. Balanced modulation is used in certain types of communications such as single side-band systems, but it is not used in standard AM broadcast systems.

EXAMPLE 17-3

Determine the frequencies contained in the output signal of the balanced modulator in Figure 17-22.

FIGURE 17-22



Solution The upper-side frequency is

$$f_c + f_m = 5 \text{ MHz} + 10 \text{ kHz} = 5.01 \text{ MHz}$$

The lower-side frequency is

$$f_c - f_m = 5 \text{ MHz} - 10 \text{ kHz} = 4.99 \text{ MHz}$$

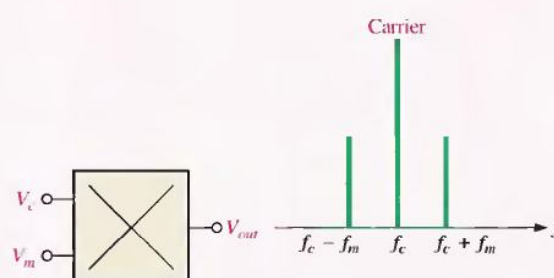
Related Problem Explain how the separation between the side frequencies can be increased using the same carrier frequency.

Standard Amplitude Modulation (AM)

In standard AM systems, the output signal contains the carrier frequency as well as the sum and difference side frequencies. The frequency spectrum in Figure 17–23 illustrates standard amplitude modulation.

► **FIGURE 17–23**

The output frequency spectrum of a standard amplitude modulator.



The expression for a standard amplitude-modulated signal is

Equation 17–3

$$V_{out} = V_{c(p)}^2 \sin 2\pi f_c t + \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi (f_c - f_m) t - \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi (f_c + f_m) t$$

Notice in Equation 17–3 that the first term is for the carrier frequency and the other two terms are for the side frequencies. Let's see how the carrier-frequency term gets into the equation.

If a dc voltage equal to the peak of the carrier voltage is added to the modulating signal before the modulating signal is multiplied by the carrier signal, a carrier-signal term appears in the final result as shown in the following steps. Add the peak carrier voltage to the modulating signal, and you get the following expression:

$$V_{c(p)} + V_{m(p)} \sin 2\pi f_m t$$

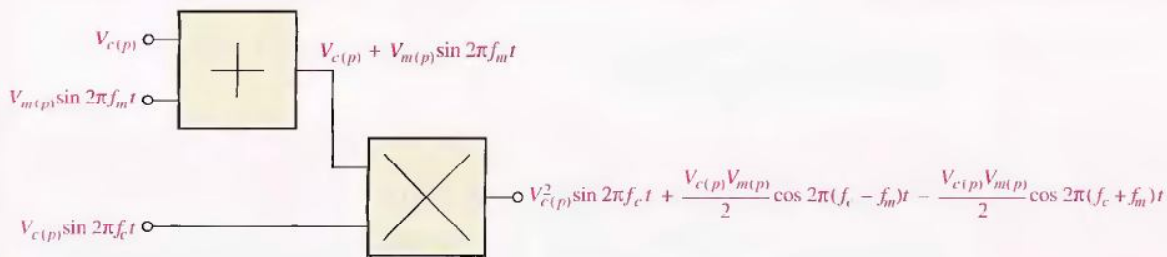
Multiply by the carrier signal.

$$\begin{aligned} V_{out} &= (V_{c(p)} \sin 2\pi f_c t)(V_{c(p)} + V_{m(p)} \sin 2\pi f_m t) \\ &= \underbrace{V_{c(p)}^2 \sin 2\pi f_c t}_{\text{carrier term}} + \underbrace{V_{c(p)} V_{m(p)} (\sin 2\pi f_c t)(\sin 2\pi f_m t)}_{\text{product term}} \end{aligned}$$

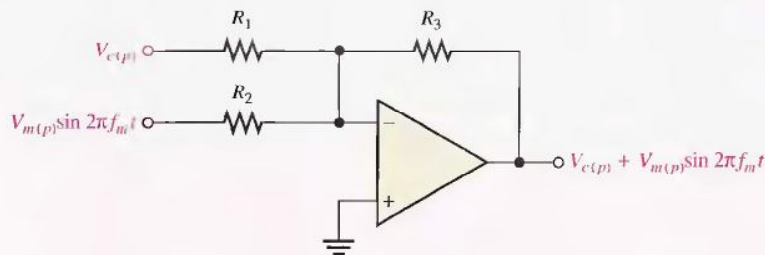
Apply the basic trigonometric identity to the product term.

$$V_{out} = V_{c(p)}^2 \sin 2\pi f_c t + \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi (f_c - f_m) t - \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi (f_c + f_m) t$$

This result shows that the output of the multiplier contains a carrier term and two side-frequency terms. Figure 17–24 illustrates how a standard amplitude modulator can be implemented by a summing circuit followed by a linear multiplier. Figure 17–25 shows a possible implementation of the summing circuit.


FIGURE 17-24

Basic block diagram of an amplitude modulator.


FIGURE 17-25

Implementation of the summing circuit in the amplitude modulator.

EXAMPLE 17-4

A carrier frequency of 1200 kHz is modulated by a sinusoidal wave with a frequency of 25 kHz by a standard amplitude modulator. Determine the output frequency spectrum.

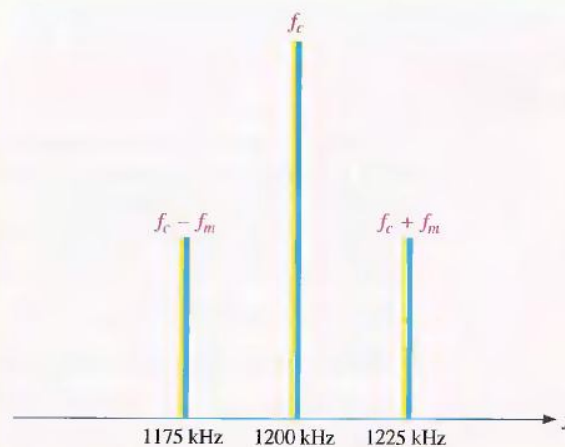
Solution The lower-side frequency is

$$f_c - f_m = 1200 \text{ kHz} - 25 \text{ kHz} = 1175 \text{ kHz}$$

The upper-side frequency is

$$f_c + f_m = 1200 \text{ kHz} + 25 \text{ kHz} = 1225 \text{ kHz}$$

The output contains the carrier frequency and the two side frequencies as shown in Figure 17-26.

FIGURE 17-26


Related Problem Compare the output frequency spectrum in this example to that of a balanced modulator having the same inputs.

Amplitude Modulation with Voice or Music

To this point in our discussion, we have considered the modulating signal to be a pure sinusoidal signal just to keep things fairly simple. If you receive an AM signal modulated by a pure sinusoidal signal in the audio frequency range, you will hear a single tone from the receiver's speaker.

An **audio** signal (voice or music) consists of many sinusoidal components within a range of frequencies from about 20 Hz to 20 kHz. For example, if a carrier frequency is amplitude modulated with voice or music with frequencies from 100 Hz to 10 kHz, the frequency spectrum is as shown in Figure 17-27. Instead of one lower-side and one upper-side frequency as in the case of a single-frequency modulating signal, a band of lower-side frequencies and a band of upper-side frequencies correspond to the sum and difference frequencies of each sinusoidal component of the voice or music signal.

FIGURE 17-27

Example of a frequency spectrum for a voice or music signal.



SECTION 17-3 REVIEW

1. What is amplitude modulation?
2. What is the difference between balanced modulation and standard AM?
3. What two input signals are used in amplitude modulation? Explain the purpose of each signal.
4. What are the upper-side frequency and the lower-side frequency?
5. How can a balanced modulator be changed to a standard amplitude modulator?

17-4 THE MIXER

The mixer in the receiver system discussed in Section 17-1 can be implemented with a linear multiplier as you will see in this section. The basic principles of linear multiplication of sinusoidal signals are covered, and you will see how sum and difference frequencies are produced. The difference frequency is a critical part of the operation of many types of receiver systems.

After completing this section, you should be able to

- Discuss the basic function of a mixer
- Explain why a mixer is a linear multiplier
- Describe the frequencies in the mixer and IF portion of a receiver

The **mixer** is basically a frequency converter because it changes the frequency of a signal to another value. The mixer in a receiver system takes the incoming modulated RF signal (which is sometimes amplified by an RF amplifier and sometimes not) along with the signal from the local oscillator and produces a modulated signal with a frequency equal to the difference of its two input frequencies (RF and LO). The mixer also produces a frequency equal to the sum of the input frequencies. The mixer function is illustrated in Figure 17-28.

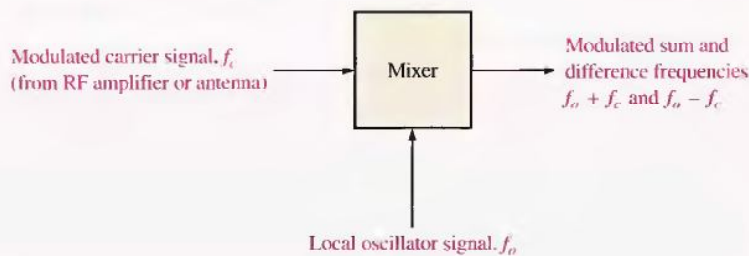


FIGURE 17-28

The mixer function.

In the case of receiver applications, the mixer must produce an output that has a frequency component equal to the difference of its input frequencies. From the mathematical analysis in Section 17-3, you can see that if two sinusoidal signals are multiplied, the product contains the difference frequency and the sum frequency. Thus, the mixer is actually a linear multiplier as indicated in Figure 17-29.

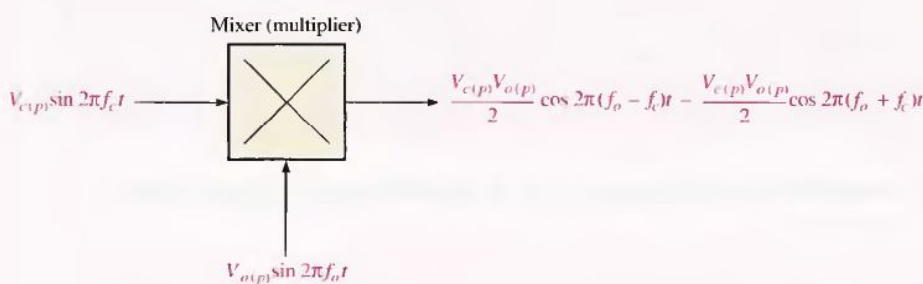


FIGURE 17-29

The mixer as a linear multiplier.

EXAMPLE 17-5

Determine the output expression for a multiplier with one sinusoidal input having a peak voltage of 5 mV and a frequency of 1200 kHz and the other input having a peak voltage of 10 mV and a frequency of 1655 kHz.

Solution The two input expressions are

$$v_1 = (5 \text{ mV}) \sin 2\pi(1200 \text{ kHz})t$$

$$v_2 = (10 \text{ mV}) \sin 2\pi(1655 \text{ kHz})t$$

Multiplying,

$$v_1 v_2 = (5 \text{ mV})(10 \text{ mV})[\sin 2\pi(1200 \text{ kHz})t][\sin 2\pi(1655 \text{ kHz})t]$$

Applying the trigonometric identity, $(\sin A)(\sin B) = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$,

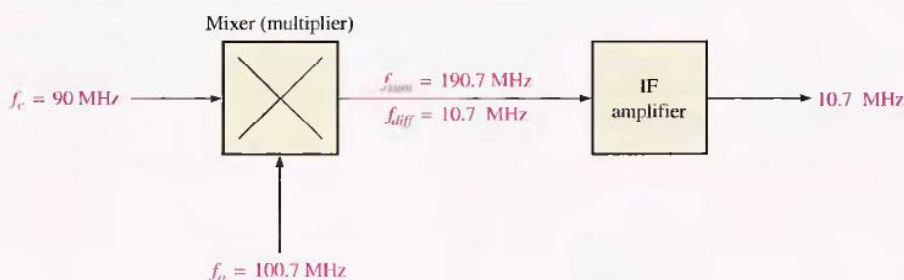
$$\begin{aligned} V_{out} &= \frac{(5 \text{ mV})(10 \text{ mV})}{2} \cos 2\pi(1655 \text{ kHz} - 1200 \text{ kHz})t \\ &\quad - \frac{(5 \text{ mV})(10 \text{ mV})}{2} \cos 2\pi(1655 \text{ kHz} + 1200 \text{ kHz})t \\ V_{out} &= (25 \mu\text{V}) \cos 2\pi(455 \text{ kHz})t - (25 \mu\text{V}) \cos 2\pi(2855 \text{ kHz})t \end{aligned}$$

Related Problem What is the value of the peak amplitude and frequency of the difference frequency component in this example?

In the receiver system, both the sum and difference frequencies from the mixer are applied to the IF (intermediate frequency) amplifier. The IF amplifier is actually a tuned amplifier that is designed to respond to the difference frequency while rejecting the sum frequency. You can think of the IF amplifier section of a receiver as a band-pass filter plus an amplifier because it uses resonant circuits to provide the frequency selectivity. This is illustrated in Figure 17-30.

► **FIGURE 17-30**

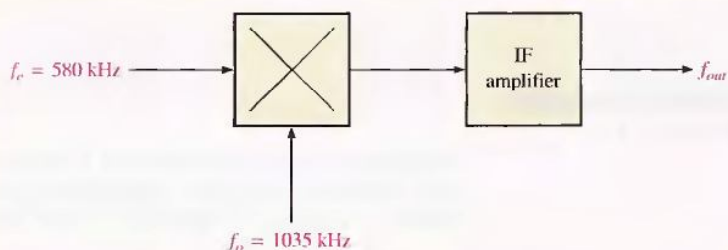
Example of frequencies in the mixer and IF portion of a receiver.



EXAMPLE 17-6

Determine the output frequency of the IF amplifier for the conditions shown in Figure 17-31.

► **FIGURE 17-31**



Solution The IF amplifier produces only the difference frequency signal on its output.

$$f_{out} = f_{diff} = f_o - f_c = 1035 \text{ kHz} - 580 \text{ kHz} = 455 \text{ kHz}$$

Related Problem Based on your basic knowledge of the superheterodyne receiver from Section 17-1, determine the IF output frequency when the incoming RF signal changes to 1550 kHz.

SECTION 17-4 REVIEW

1. What is the purpose of the mixer in a superheterodyne receiver?
2. How does the mixer produce its output?
3. If a mixer has 1000 kHz on one input and 350 kHz on the other, what frequencies appear on the output?

17-5 AM DEMODULATION

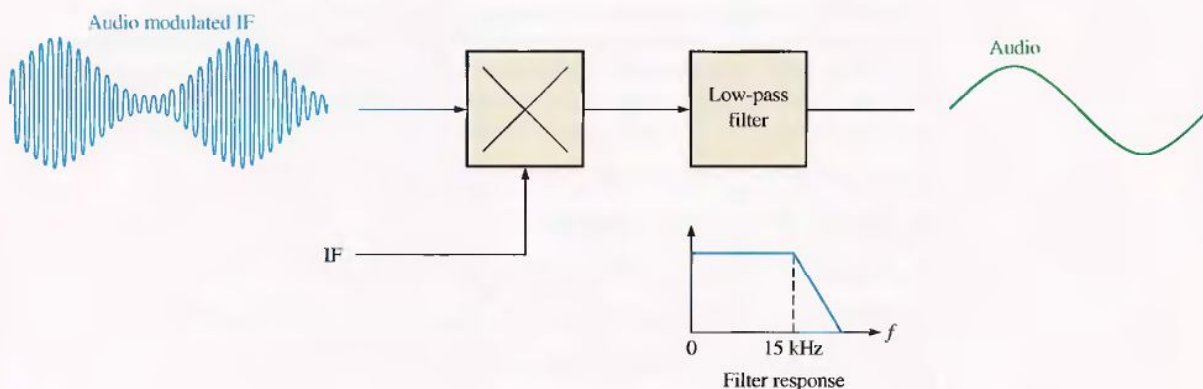
The linear multiplier can be used to demodulate or detect an AM signal as well as to perform the modulation process that was discussed in Section 17-3. Demodulation can be thought of as reverse modulation. The purpose is to get back the original modulating signal (sound in the case of standard AM receivers). The detector in the AM receiver can be implemented using a multiplier, although another method using peak envelope detection is common.

After completing this section, you should be able to

- Describe AM demodulation
- Discuss a basic AM demodulator
- Discuss the frequency spectra

The Basic AM Demodulator

An AM demodulator can be implemented with a linear multiplier followed by a low-pass filter, as shown in Figure 17-32. The critical frequency of the filter is the highest audio frequency that is required for a given application (15 kHz, for example).



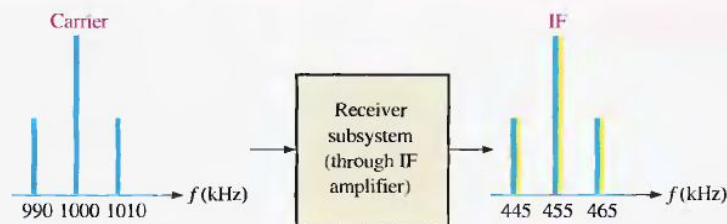
▲ FIGURE 17-32
Basic AM demodulator.

Operation in Terms of the Frequency Spectra

Let's assume a carrier modulated by a single tone with a frequency of 10 kHz is received and converted to a modulated intermediate frequency of 455 kHz, as indicated by the frequency spectra in Figure 17-33. Notice that the upper-side and lower-side frequencies are separated from both the carrier and the IF by 10 kHz.

★ FIGURE 17-33

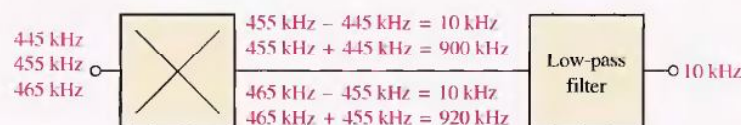
An AM signal converted to IF.



When the modulated output of the IF amplifier is applied to the demodulator along with the IF, sum and difference frequencies for each input frequency are produced as shown in Figure 17-34. Only the 10 kHz audio frequency is passed by the filter. A drawback to this type of AM detection is that a pure IF must be produced to mix with the modulated IF.

★ FIGURE 17-34

Example of demodulation.



SECTION 17-5 REVIEW

1. What is the purpose of the filter in the linear multiplier demodulator?
2. If a 455 kHz IF modulated by a 1 kHz audio frequency is demodulated, what frequency or frequencies appear on the output of the demodulator?

17-6 IF AND AUDIO AMPLIFIERS

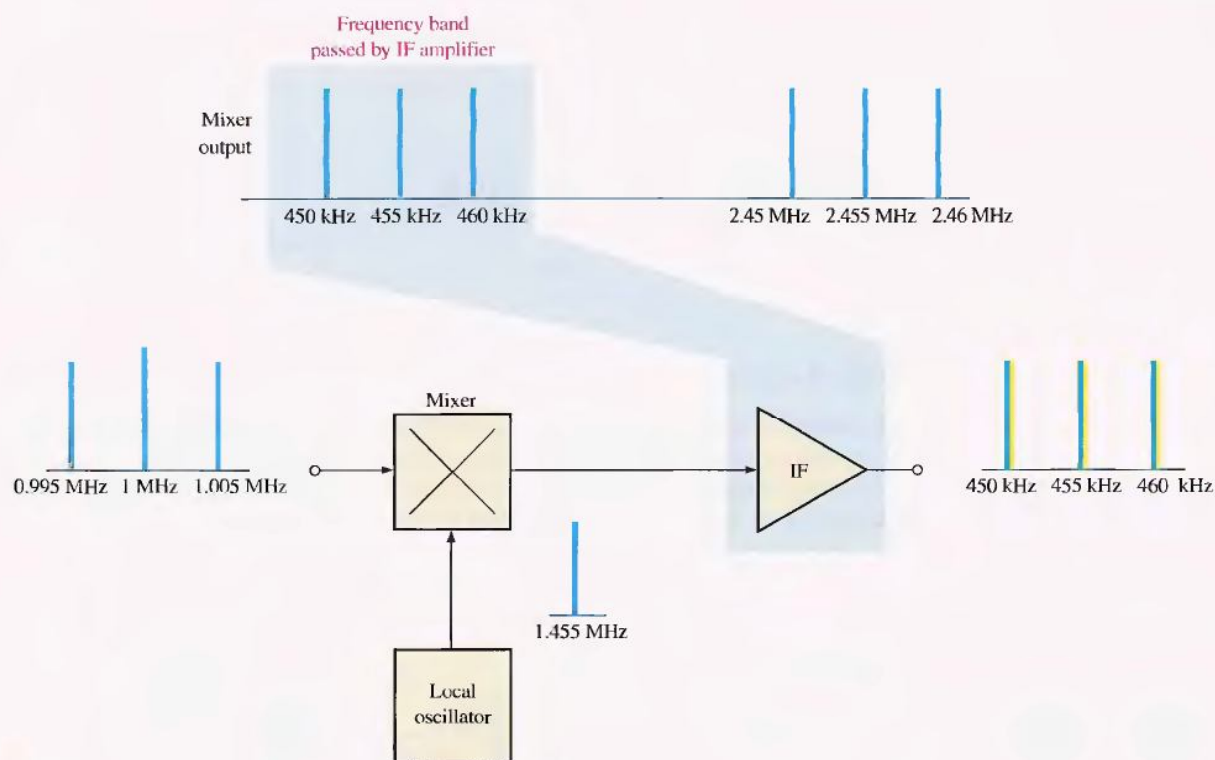
In this section, amplifiers for intermediate and audio frequencies are introduced. A typical IF amplifier is discussed and audio preamplifiers and power amplifiers are covered. As you have learned, the IF amplifier in a communications receiver provides amplification of the modulated IF signal out of the mixer before it is applied to the detector. After the audio signal is recovered by the detector, it goes to the audio preamp where it is amplified and applied to the power amplifier that drives the speaker.

After completing this section, you should be able to

- Describe IF and audio amplifiers
- Discuss the function of an IF amplifier
- Explain how the local oscillator and mixer operate with the IF amplifier
- State the purpose of the audio amplifier
- Discuss the LM386 audio power amplifier

IF Amplifiers

The IF amplifier in a receiver is a tuned amplifier with a specified bandwidth operating at a center frequency of 455 kHz for AM and 10.7 MHz for FM. The IF amplifier is one of the key features of a superheterodyne receiver because it is set to operate at a single resonant frequency that remains the same over the entire band of carrier frequencies that can be received. Figure 17-35 illustrates the basic function of an IF amplifier in terms of the frequency spectra.



▲ **FIGURE 17-35**

An illustration of the basic function of the IF amplifier in an AM receiver.

Assume, for example, that the received carrier frequency of $f_c = 1$ MHz is modulated by an audio signal with a maximum frequency of $f_m = 5$ kHz, indicated in Figure 17-35 by the frequency spectrum on the input to the mixer. For this frequency, the local oscillator is at a frequency of

$$f_o = 1 \text{ MHz} + 455 \text{ kHz} = 1.455 \text{ MHz}$$

The mixer produces the following sum and difference frequencies as indicated in Figure 17-35.

$$f_o + f_c = 1.455 \text{ MHz} + 1 \text{ MHz} = 2.455 \text{ MHz}$$

$$f_o - f_c = 1.455 \text{ MHz} - 1 \text{ MHz} = 455 \text{ kHz}$$

$$f_o + (f_c + f_m) = 1.455 \text{ MHz} + 1.005 \text{ MHz} = 2.46 \text{ MHz}$$

$$f_o + (f_c - f_m) = 1.455 \text{ MHz} + 0.995 \text{ MHz} = 2.45 \text{ MHz}$$

$$f_o - (f_c + f_m) = 1.455 \text{ MHz} - 1.005 \text{ MHz} = 450 \text{ kHz}$$

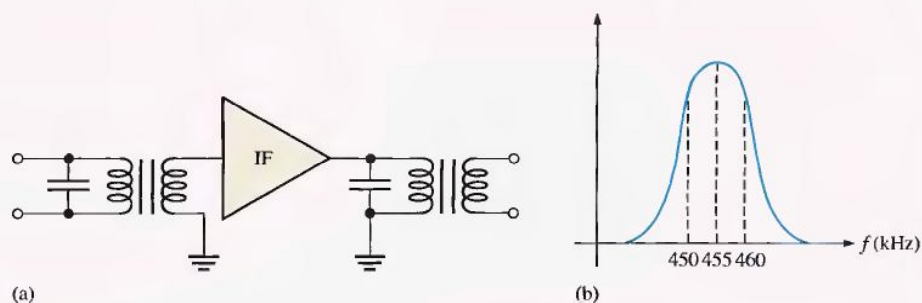
$$f_o - (f_c - f_m) = 1.455 \text{ MHz} - 0.995 \text{ MHz} = 460 \text{ kHz}$$

Since the IF amplifier is a frequency-selective circuit, it responds only to 455 kHz and any side frequencies lying in the 10 kHz band centered at 455 kHz. All of the frequencies out of the mixer are rejected except the 455 kHz IF, all lower-side frequencies down to 450 kHz, and all upper-side frequencies up to 460 kHz. This frequency spectrum is the audio modulated intermediate frequency.

Although the detailed circuitry of the IF amplifier may differ from one system to another, it always has a tuned (resonant) circuit on the input or on the output or on both. Figure 17-36(a) shows a basic IF amplifier with tuned transformer coupling at the input and output. The general frequency response curve is shown in Figure 17-36(b).

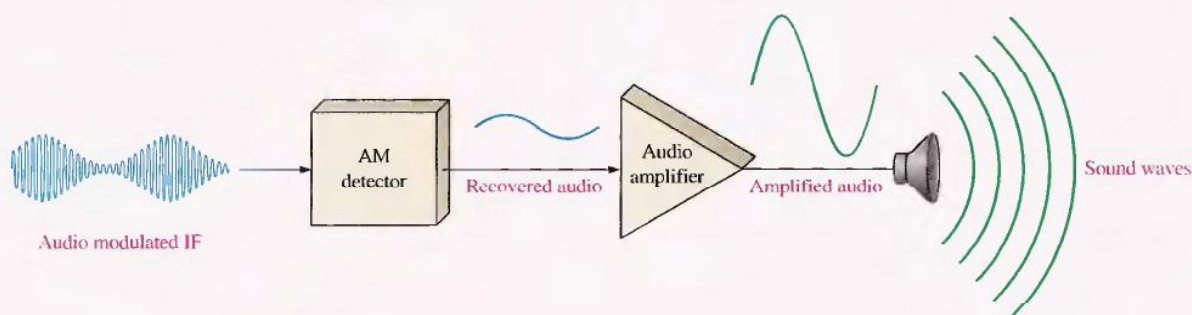
▶ **FIGURE 17-36**

A basic IF amplifier with a tuned circuit on the input and output.



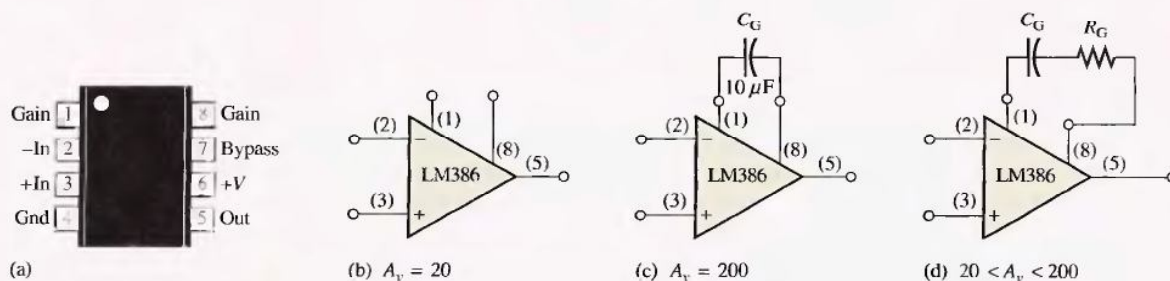
Audio Amplifiers

Audio amplifiers are used in a receiver system following the detector to provide amplification of the recovered audio signal and audio power to drive the speaker(s), as indicated in Figure 17-37. Audio amplifiers typically have bandwidths of 3 kHz to 15 kHz depending on the requirements of the system. IC audio amplifiers are available with a range of capabilities.

▶ **FIGURE 17-37**

The audio amplifier in a receiver system.

The LM386 Audio Power Amplifier This device is an example of a low-power audio amplifier that is capable of providing several hundred milliwatts to an $8\ \Omega$ speaker. It operates from any dc supply voltage in the 4 V to 12 V range, making it a good choice for battery operation. The pin configuration of the LM386 is shown in Figure 17-38(a). The voltage gain of the LM386 is 20 without external connections to the gain terminals, as shown in Figure 17-38(b). A voltage gain of 200 is achieved by connecting a $10\ \mu\text{F}$ capacitor from pin 1 to pin 8, as shown in Figure 17-38(c). Voltage gains between 20 and 200 can be realized by a resistor (R_G) and capacitor (C_G) connected in series from pin 1 to pin 8 as shown in Figure 17-38(d). These external components are effectively placed in parallel with an internal gain-setting resistor.

▶ **FIGURE 17-38**

Pin configuration and gain connections for the LM386 audio amplifier.

A typical application of the LM386 as a power amplifier in a radio receiver is shown in Figure 17-39. Here the detected AM signal is fed to the inverting input through the volume control potentiometer, R_1 , and resistor R_2 . C_1 is the input coupling capacitor and C_2 is the power supply decoupling capacitor. R_2 and C_3 filter out any residual RF or IF signal that may be on the output of the detector. R_3 and C_6 provide additional filtering before the audio signal is applied to the speaker through the coupling capacitor C_7 .

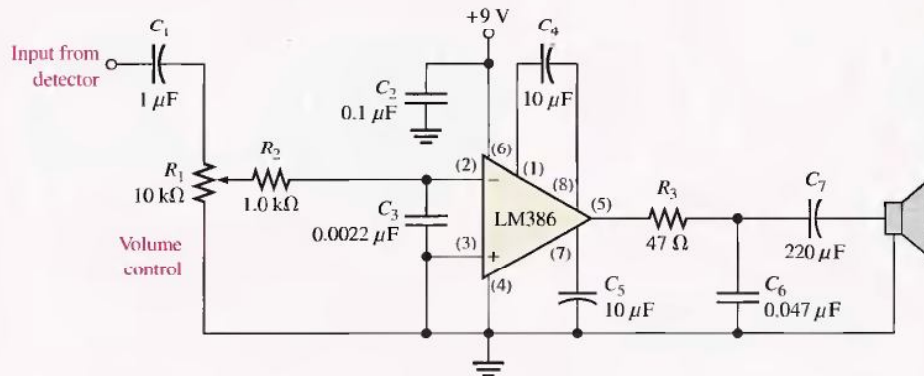


FIGURE 17-39

The LM386 as an AM audio power amplifier.

SECTION 17-6 REVIEW

1. What is the purpose of the IF amplifier in an AM receiver?
2. What is the center frequency of an AM IF amplifier?
3. Why is the bandwidth of an AM receiver IF amplifier 10 kHz?
4. Why must the audio amplifier follow the detector in a receiver system?
5. Compare the frequency response of the IF amplifier to that of the audio amplifier.

17-7 FREQUENCY MODULATION

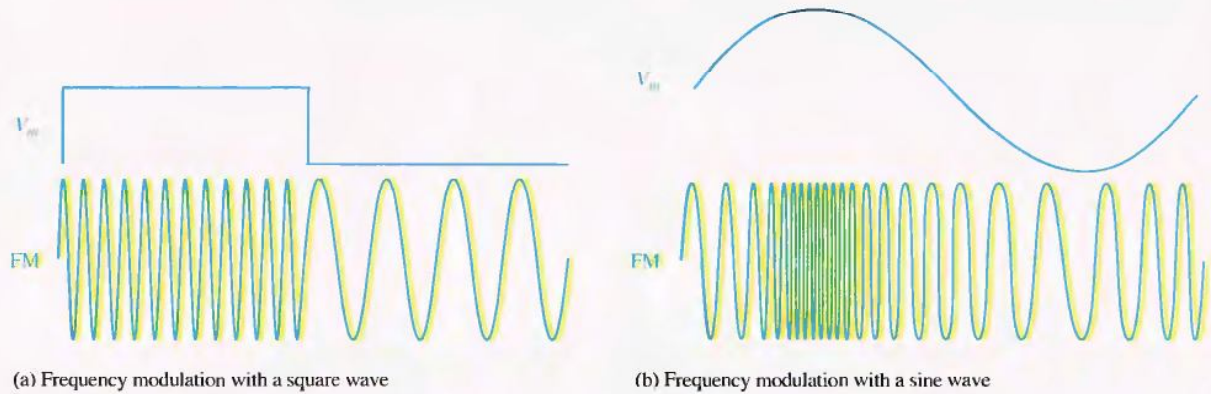
As you have seen, modulation is the process of varying a parameter of a carrier signal with an information signal. Recall that in amplitude modulation the parameter of amplitude is varied. In frequency modulation (FM), the frequency of a carrier is varied above and below its normal or at-rest value by a modulating signal. This section provides a further look into FM and discusses the differences between an AM and an FM receiver.

After completing this section, you should be able to

- Describe frequency modulation
- Discuss the voltage-controlled oscillator
- Explain frequency demodulation

In a frequency-modulated (FM) signal, the carrier frequency is increased or decreased according to the modulating signal. The amount of deviation above or below the carrier frequency depends on the amplitude of the modulating signal. The rate at which the frequency deviation occurs depends on the frequency of the modulating signal.

Figure 17-40 illustrates both a square wave and a sine wave modulating the frequency of a carrier. The carrier frequency is highest when the modulating signal is at its maximum positive amplitude and is lowest when the modulating signal is at its maximum negative amplitude.



▲ **FIGURE 17-40**

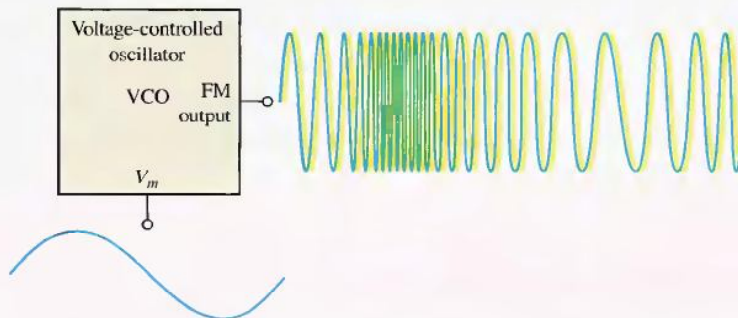
Examples of frequency modulation.

A Basic Frequency Modulator

Frequency modulation is achieved by varying the frequency of an oscillator with the modulating signal. A voltage-controlled oscillator (VCO) is typically used for this purpose, as illustrated in Figure 17-41.

► **FIGURE 17-41**

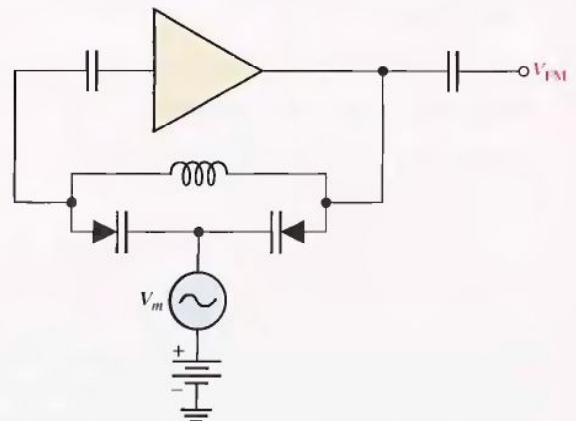
Frequency modulation with a voltage-controlled oscillator.



Generally, a variable-reactance type of voltage-controlled oscillator is used in FM applications. The variable-reactance VCO uses the varactor diode as a voltage-variable capacitance, as illustrated in Figure 17-42, where the capacitance is varied with the modulating voltage. V_m

► **FIGURE 17-42**

Basic variable-reactance VCO.



FM Demodulation

Except for the higher frequencies, the standard broadcast FM receiver is basically the same as the AM receiver up through the IF amplifier. The main difference between an FM receiver and an AM receiver, other than the frequency band, is the method used to recover the audio signal from the modulated IF.

There are several methods for demodulating an FM signal. These include slope detection, phase-shift discrimination, ratio detection, quadrature detection, and phase-locked loop demodulation. Most of these methods are covered in detail in communications courses. However, because of its importance in many types of applications, we will cover the phase-locked loop (PLL) demodulation in the next section.

SECTION 17-7 REVIEW

1. How does an FM signal carry information?
2. On what principle are most VCOs used in FM based?

17-8 THE PHASE-LOCKED LOOP (PLL)

In the last section, the PLL was mentioned as a way to demodulate an FM signal. In addition to FM demodulation, PLLs are used in a wide variety of communications applications, which include TV receivers, tone decoders, telemetry receivers, modems, and data synchronizers, to name a few. Many of these applications are covered in electronic communications courses. In fact, entire books have been written on the finer points of PLL operation, analysis, and applications. The approach in this section is intended only to present the basic concept and give you an intuitive idea of how PLLs work and how they are used in FM demodulation. A specific PLL integrated circuit is also introduced.

After completing this section, you should be able to

- Describe a phase-locked loop (PLL)
- Draw a basic block diagram for the PLL
- Discuss the phase detector and state its purpose
- State the purpose of the VCO
- State the purpose of the low-pass filter
- Explain lock range and capture range
- Discuss the LM565 PLL and explain how it can be used as an FM demodulator

The Basic PLL Concept

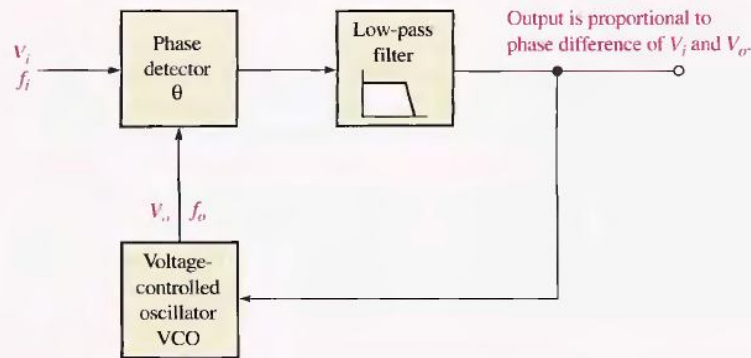
The **phase-locked loop (PLL)** is a feedback circuit consisting of a phase detector, a low pass filter, and a voltage-controlled oscillator (VCO). Some PLLs also include an amplifier in the loop, and in some applications the filter is not used.

The PLL is capable of locking onto or synchronizing with an incoming signal. When the phase of the incoming signal changes, indicating a change in frequency, the phase detector's output increases or decreases just enough to keep the VCO frequency the same as the frequency of the incoming signal. A basic PLL block diagram is shown in Figure 17-43.



► FIGURE 17-43

Basic PLL block diagram.



The general operation of a PLL is as follows. The phase detector compares the phase difference between the incoming signal, V_i , and the VCO signal, V_o . When the frequency of the incoming signal, f_i , is different from that of the VCO frequency, f_o , the phase angle between the two signals is also different. The output of the phase detector and the filter is proportional to the phase difference of the two signals. This proportional voltage is fed to the VCO, forcing its frequency to move toward the frequency of the incoming signal until the two frequencies are equal. At this point, the PLL is locked onto the incoming frequency. If f_i changes, the phase difference also changes, forcing the VCO to track the incoming frequency.

The Phase Detector

The phase-detector circuit in a PLL is basically a linear multiplier. The following analysis illustrates how it works in a PLL application. The incoming signal, V_i , and the VCO signal, V_o , applied to the phase detector can be expressed as

$$v_i = V_i \sin(2\pi f_i t + \theta_i)$$

$$v_o = V_o \sin(2\pi f_o t + \theta_o)$$

where θ_i and θ_o are the relative phase angles of the two signals. The phase detector multiplies these two signals and produces a sum and difference frequency output, V_d , as follows:

$$V_d = V_i \sin(2\pi f_i t + \theta_i) \times V_o \sin(2\pi f_o t + \theta_o)$$

$$= \frac{V_i V_o}{2} \cos[2\pi f_i t + \theta_i - (2\pi f_o t + \theta_o)] - \frac{V_i V_o}{2} \cos[(2\pi f_i t + \theta_i) + (2\pi f_o t + \theta_o)]$$

When the PLL is locked,

$$f_i = f_o$$

and

$$2\pi f_i t = 2\pi f_o t$$

Therefore, the detector output voltage is

$$V_d = \frac{V_i V_o}{2} [\cos(\theta_i - \theta_o) - \cos(4\pi f_i t + \theta_i + \theta_o)]$$

The second cosine term in the above equation is a second harmonic term ($2 \times 2\pi f_i t$) and is filtered out by the low-pass filter.

The control voltage on the output of the filter is expressed as

$$V_c = \frac{V_i V_o}{2} \cos \theta_e$$

Equation 17-4

where $\theta_e = \theta_i - \theta_o$, where θ_e is the *phase error*. The filter output voltage is proportional to the phase difference between the incoming signal and the VCO signal and is used as the control voltage for the VCO. This operation is illustrated in Figure 17-44.

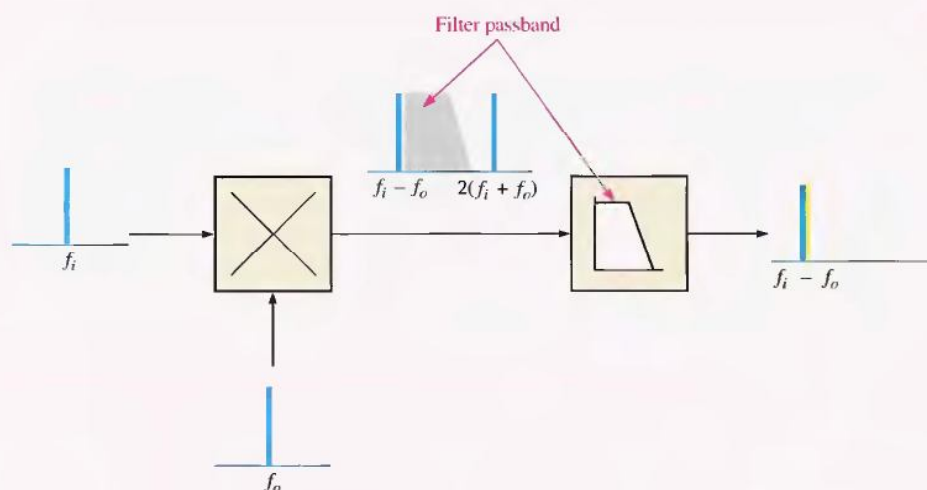


FIGURE 17-44

Basic phase detector/filter operation.

EXAMPLE 17-7

A PLL is locked onto an incoming signal with a frequency of 1 MHz at a phase angle of 50° . The VCO signal is at a phase angle of 20° . The peak amplitude of the incoming signal is 0.5 V and that of the VCO output signal is 0.7 V.

- What is the VCO frequency?
- What is the value of the control voltage being fed back to the VCO at this point?

Solution

(a) Since the PLL is in lock, $f_i = f_o = 1 \text{ MHz}$.

(b) $\theta_e = \theta_i - \theta_o = 50^\circ - 20^\circ = 30^\circ$

$$V_c = \frac{V_i V_o}{2} \cos \theta_e = \frac{(0.5 \text{ V})(0.7 \text{ V})}{2} \cos 30^\circ = (0.175 \text{ V}) \cos 30^\circ = \mathbf{0.152 \text{ V}}$$

Related Problem

If the phase angle of the incoming signal changes instantaneously to 30° , indicating a change in frequency, what is the instantaneous VCO control voltage?

The Voltage-Controlled Oscillator (VCO)

Voltage-controlled oscillators can take many forms. A VCO can be some type of *LC* or crystal oscillator, or it can be some type of *RC* oscillator or multivibrator. No matter the exact type, most VCOs employed in PLLs operate on the principle of *variable reactance* using the varactor diode as a voltage-variable capacitor.

The capacitance of a varactor diode varies inversely with reverse-bias voltage. The capacitance decreases as reverse voltage increases and vice versa.

In a PLL, the control voltage fed back to the VCO is applied as a reverse-bias voltage to the varactor diode within the VCO. The frequency of oscillation is inversely related to capacitance for an RC type oscillator by the formula

$$f_o = \frac{1}{2\pi RC}$$

and for an LC type oscillator by the formula

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

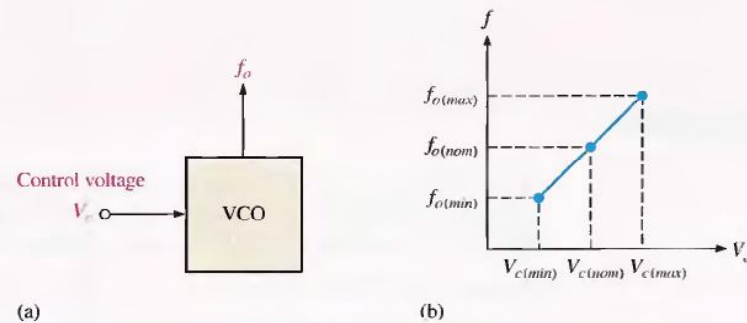
These formulas show that frequency increases as capacitance decreases and vice versa.

Capacitance decreases as reverse voltage (control voltage) increases. Therefore, an increase in control voltage to the VCO causes an increase in frequency and vice versa. Basic VCO operation is illustrated in Figure 17-45. The graph in part (b) shows that at the nominal control voltage, $V_{c(nom)}$, the oscillator is running at its nominal or free-running frequency, $f_{o(nom)}$. An increase in V_c above the nominal value forces the oscillator frequency to increase, and a decrease in V_c below the nominal value forces the oscillator frequency to decrease. There are, of course, limits on the operation as indicated by the minimum and maximum points. The transfer function or conversion gain, K , of the VCO is normally expressed as a certain frequency deviation per unit change in control voltage.

$$K = \frac{\Delta f_o}{\Delta V_c}$$

► **FIGURE 17-45**

Basic VCO operation.



EXAMPLE 17-8

The output frequency of a certain VCO changes from 50 kHz to 65 kHz when the control voltage increases from 0.5 V to 1 V. What is the conversion gain, K ?

Solution

$$K = \frac{\Delta f_o}{\Delta V_c} = \frac{65 \text{ kHz} - 50 \text{ kHz}}{1 \text{ V} - 0.5 \text{ V}} = \frac{15 \text{ kHz}}{0.5 \text{ V}} = 30 \text{ kHz/V}$$

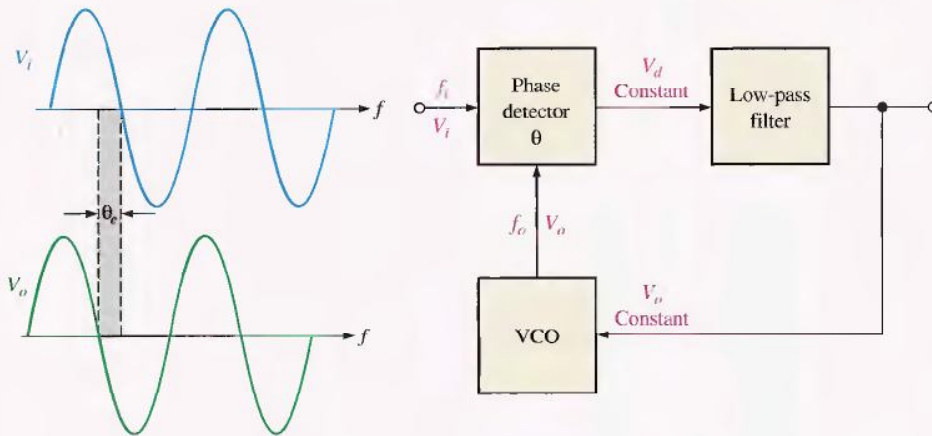
Related Problem

If the conversion gain of a certain VCO is 20 kHz/V, how much frequency deviation does a change in control voltage from 0.8 V to 0.5 V produce? If the VCO frequency is 250 kHz at 0.8 V, what is the frequency at 0.5 V?

Basic PLL Operation

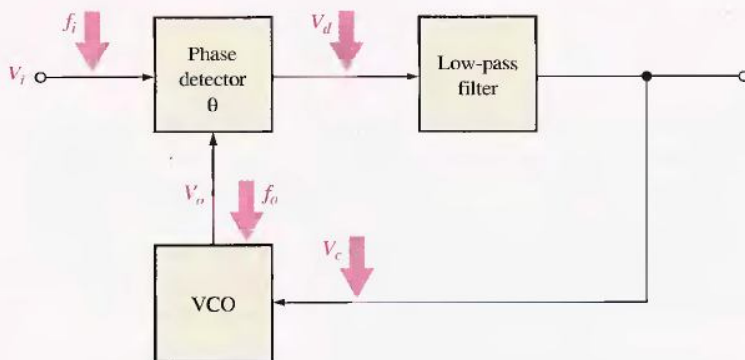
When the PLL is locked, the incoming frequency, f_i , and the VCO frequency, f_o , are equal. However, there is always a phase difference between them called the *static phase error*. The phase error, θ_e , is the parameter that keeps the PLL locked in. As you have seen, the filtered voltage from the phase detector is proportional to θ_e (Equation 17-4). This voltage controls the VCO frequency and is always just enough to keep $f_o = f_i$.

Figure 17-46 shows the PLL and two sinusoidal signals of the same frequency but with a phase difference, θ_e . For this condition the PLL is in lock and the VCO control voltage is constant. If f_i decreases, θ_e increases to θ_{e1} as illustrated in Figure 17-47. This increase in θ_e is sensed by the phase detector causing the VCO control voltage to decrease, thus decreasing f_o until $f_o = f_i$ and keeping the PLL in lock. If f_i increases, θ_e decreases to θ_{e1} as illustrated in Figure 17-48. This decrease in θ_e causes the VCO control voltage to increase, thus increasing f_o until $f_o = f_i$ and keeping the PLL in lock.



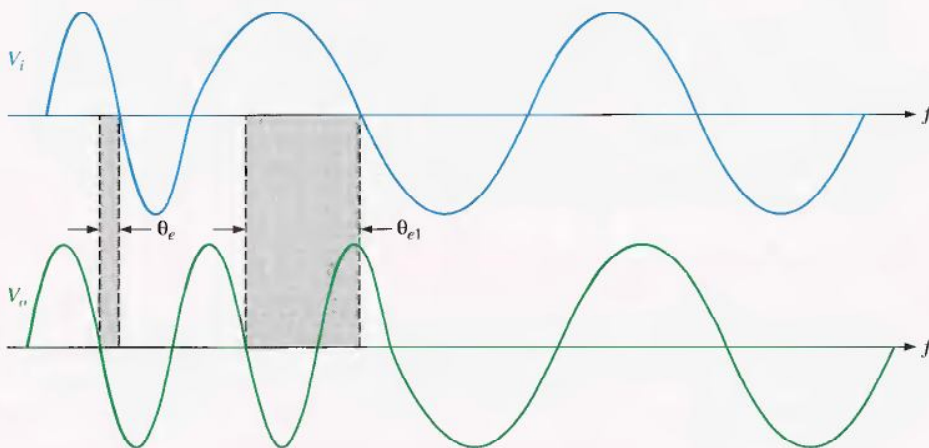
◀ **FIGURE 17-46**

PLL in lock under static condition ($f_o = f_i$ and constant θ_e).

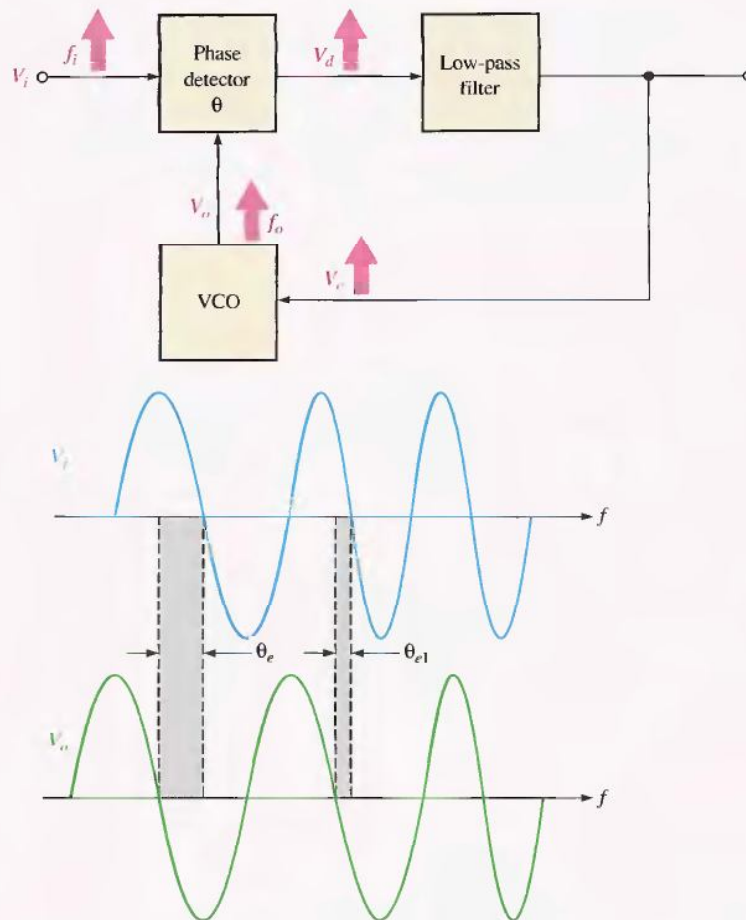


◀ **FIGURE 17-47**

PLL action when f_i decreases.



► FIGURE 17-48

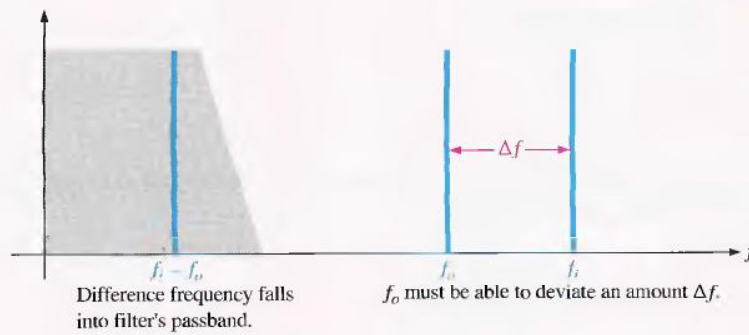
PLL action when f_i increases.

Lock Range Once the PLL is locked, it will track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock is called the **lock range** or tracking range. Limitations on the hold-in range are the maximum frequency deviations of the VCO and the output limits of the phase detector. The hold-in range is independent of the bandwidth of the low-pass filter because, when the PLL is in lock, the difference frequency ($f_i - f_o$) is zero or a very low instantaneous value that falls well within the bandwidth. The hold-in range is usually expressed as a percentage of the VCO frequency.

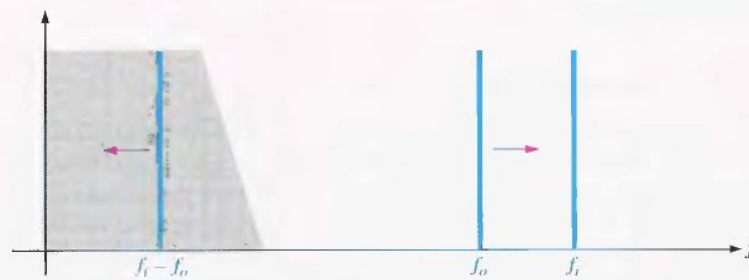
Capture Range Assuming the PLL is not in lock, the range of frequencies over which it can acquire lock with an incoming signal is called the **capture range**. Two basic conditions are required for a PLL to acquire lock. First, the difference frequency ($f_o - f_i$) must be low enough to fall within the filter's bandwidth. This means that the incoming frequency must not be separated from the nominal or free-running frequency of the VCO by more than the bandwidth of the low-pass filter. Second, the maximum deviation, Δf_{max} , of the VCO frequency must be sufficient to allow f_o to increase or decrease to a value equal to f_i . These conditions are illustrated in Figure 17-49; and when they exist, the PLL will "pull" the VCO frequency toward the incoming frequency until $f_o = f_i$.

The LM565 Phase-Locked Loop

The LM565 is a good example of an integrated circuit PLL. The circuit consists of a VCO, a phase detector, a low-pass filter formed by an internal resistor and an external capacitor, and an amplifier. The free-running VCO frequency can be set with external components. A block diagram is shown in Figure 17-50. The LM565 can be used for the frequency range from 0.001 Hz to 500 kHz.



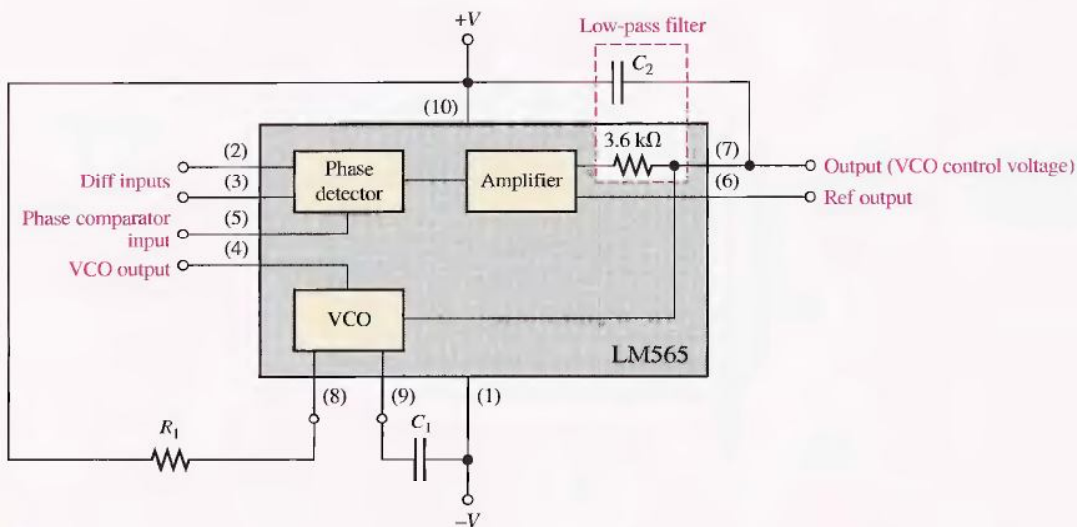
(a)

(b) $f_i - f_o$ decreases as f_o deviates towards f_i .

The free-running frequency of the VCO is set by the values of R_1 and C_1 in Figure 17-50 according to the following formula. The frequency is in hertz when the resistance is in ohms and the capacitance is in farads.

$$f_o \cong \frac{1.2}{4R_1C_1}$$

Equation 17-5



▲ FIGURE 17-50

Block diagram of the LM565 PLL.

The lock range is given by

Equation 17-6

$$f_{lock} = \pm \frac{8f_o}{V_{CC}}$$

where V_{CC} is the total voltage between the positive and negative dc supply voltage terminals.

The capture range is given by

Equation 17-7

$$f_{cap} \cong \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_{lock}}{(3600 \Omega)C_2}}$$

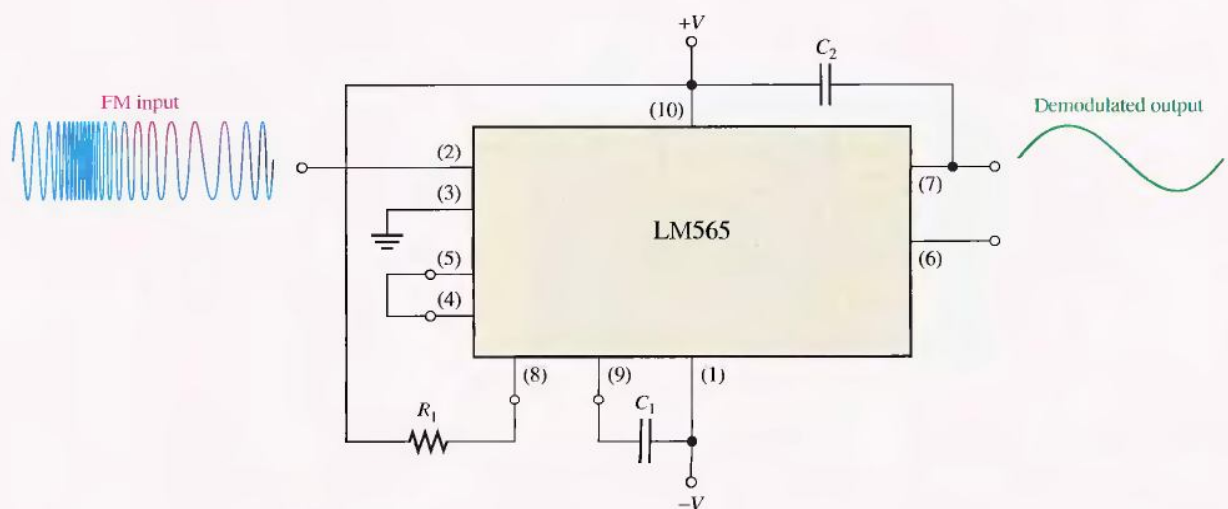
The 3600 is the value of the internal filter resistor in ohms. You can see that the capture range is dependent on the filter bandwidth as determined by the internal resistor and the external capacitor C_2 .

The PLL as an FM Demodulator

As you have seen, the VCO control voltage in a PLL depends on the deviation of the incoming frequency. The PLL will produce a voltage proportional to the frequency of the incoming signal which, in the case of FM, is the original modulating signal.

Figure 17-51 shows a typical connection for the LM565 as an FM demodulator. If the IF input is frequency modulated by a sinusoidal signal, you get a sinusoidal signal on the output as indicated. Since the maximum operating frequency is 500 kHz, this device must be used in double-conversion FM receivers. A double-conversion FM receiver is one in which essentially two mixers are used to first convert the RF to a 10.7 MHz IF and then convert this to a 455 kHz IF.

The free-running frequency of the VCO is adjusted to approximately 455 kHz, which is the center of the modulated IF range. C_1 can be any value, but R_1 should be in the range from 2 k Ω to 20 k Ω . The input can be directly coupled as long as there is no dc voltage difference between pins 2 and 3. The VCO is connected to the phase detector by an external wire between pins 4 and 5.



▲ FIGURE 17-51

The LM565 as an FM demodulator.

EXAMPLE 17-9

Determine the values for R_1 , C_1 , and C_2 for the LM565 in Figure 17-51 for a free-running frequency of 455 kHz and a capture range of ± 10 kHz. The dc supply voltages are ± 6 V.

Solution Use Equation 17-5 to calculate C_1 . Choose $R_1 = 4.7 \text{ k}\Omega$.

$$f_o \cong \frac{1.2}{4R_1C_1}$$

$$C_1 \cong \frac{1.2}{4R_1f_o} = \frac{1.2}{4(4700 \Omega)(455 \times 10^3 \text{ Hz})} = 140 \times 10^{-12} \text{ F} = \mathbf{140 \text{ pF}}$$

The lock range must be determined before you can calculate C_2 .

$$f_{\text{lock}} = \pm \frac{8f_o}{V_{\text{CC}}} = \pm \frac{8(455 \text{ kHz})}{12 \text{ V}} = \pm 303 \text{ kHz}$$

Use Equation 17-7 to calculate C_2 .

$$f_{\text{cap}} \cong \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_{\text{lock}}}{(3600 \Omega)C_2}}$$

$$f_{\text{cap}}^2 \cong \left(\frac{1}{2\pi}\right)^2 \frac{2\pi f_{\text{lock}}}{(3600 \Omega)C_2}$$

$$C_2 \cong \left(\frac{1}{2\pi}\right)^2 \frac{2\pi f_{\text{lock}}}{(3600 \Omega)f_{\text{cap}}^2} = \left(\frac{1}{2\pi}\right)^2 \frac{2\pi(303 \times 10^3 \text{ Hz})}{(3600 \Omega)(10 \times 10^3 \text{ Hz})^2}$$

$$= 0.134 \times 10^{-6} \text{ F} = \mathbf{0.134 \mu\text{F}}$$

Related Problem What can you do to increase the capture range from ± 10 kHz to ± 15 kHz?

**SECTION 17-8
REVIEW**

1. List the three basic components in a phase-locked loop.
2. What is another circuit used in some PLLs other than the three listed in Question 1?
3. What is the basic function of a PLL?
4. What is the difference between the lock range and the capture range of a PLL?
5. Basically, how does a PLL track the incoming frequency?



SYSTEM APPLICATION

The DCE (data communications equipment) system introduced at the opening of this chapter includes an FSK (frequency shift keying) modem (modulator/demodulator). FSK is one method for modulating digital data for transmission over voice phone lines and is basically a form of frequency modulation. In this system application, the focus is on the low-speed modulator/demodulator (modem) board, which is implemented with a VCO for transmitting FSK signals and a PLL for receiving FSK signals.

A Brief Description of the System

The FSK modem interfaces a computer with the telephone network so that digital data, which are incompatible with the standard phone system because of bandwidth limitations, can be transmitted and received over regular phone lines, thus allowing computers to communicate with each other. Figure 17-52 shows a diagram of a simple data communications system in which a modem at each end of the phone line provides interfacing for a computer.

The modem (DCE) consists of three basic functional blocks as shown in Figure 17-53: the FSK modem circuits, the phone line interface circuits, and the timing and control circuits. The dual-polarity power supply is not shown. Although the focus of this system application is the FSK modem board, we will briefly look at each of the other parts to give you a basic idea of the overall system function.

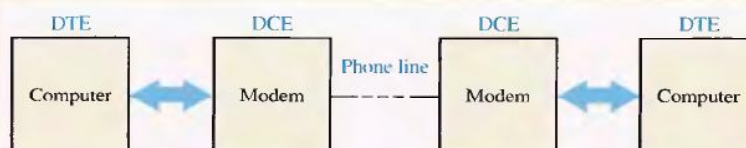
The Phone Line Interface The main purposes of this circuitry are to couple the phone line to the modem by proper impedance matching, to provide necessary filtering, and to accommodate full-duplex transmission of data. *Full-duplex* means essentially that information can be going both ways on a single phone line at the same time. This allows a computer, connected to a modem, to be sending data and receiving data simultaneously without the transmitted data interfering with the received data. Full-duplexing is implemented by assigning the transmitted data one bandwidth and the received data another separate bandwidth within the 300 Hz to 3 kHz overall bandwidth of the phone network.

Timing and Control One basic function of the timing and control circuits is to determine the proper mode of operation for the modem. The two modes are the originate mode and the answer mode. Another function is to provide a standard interface (such as RS-232C) with the DTE (computer). The RS-232C standard requires certain defined command and control signals, data signals, and voltage levels for each signal.

Digital Data Before we get into FSK, let's briefly review digital data. A detailed knowledge of binary numbers is not necessary for this system application. Information is represented in digital form by 1s and 0s, which are the binary digits or bits. In terms of voltage waveforms, a 1 is generally represented by a high level and a 0 by a low level. A stream of serial data consists of a sequence of bits as illustrated by an example in Figure 17-54(a).

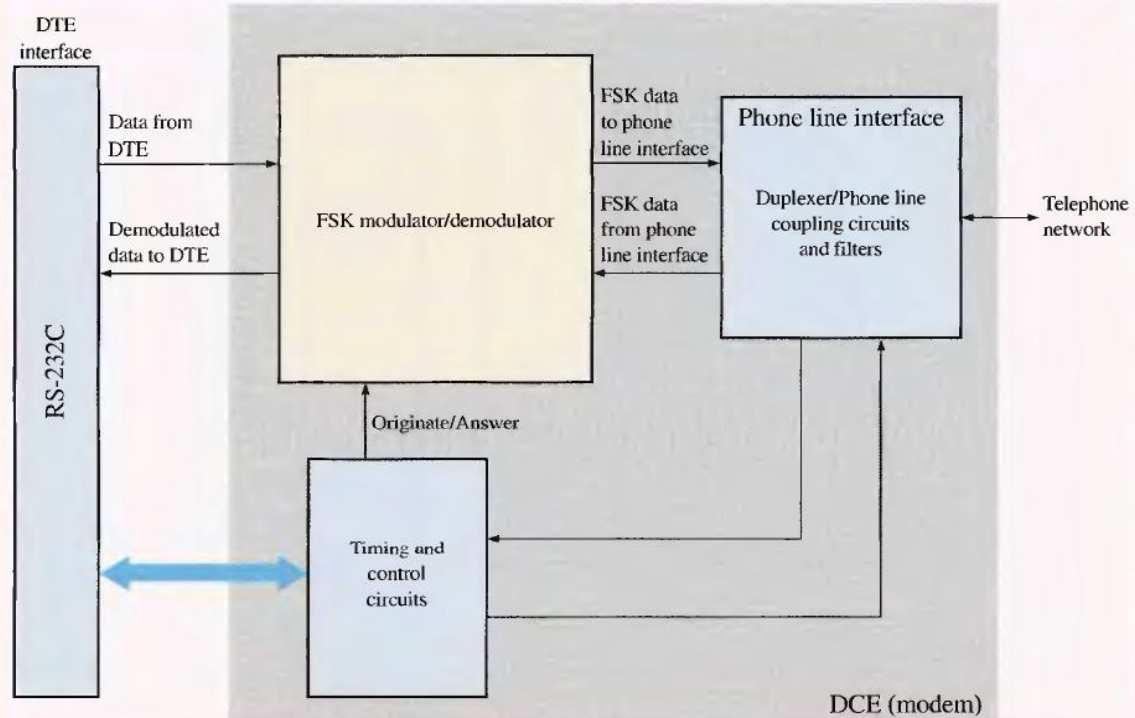
Baud Rate The baud rate is the number of bits/s of the transmitted data. This can be determined by taking the reciprocal of the time of the shortest pulse transmitted. A low-speed modem, such as the one we are focusing on, sends and receives digital data at a rate of 300 bits/s or 300 baud. For example, if we have an alternating sequence of 1s and 0s (highs and lows), as indicated in Figure 17-54(b), each bit takes 3.33 ms. This is the minimum time for a pulse in the data stream, so the baud rate is $1/3.33 \text{ ms} = 300 \text{ baud}$. Since it takes two bits, a 1 and a 0, to make up the period of this particular waveform, the fundamental frequency of this format is $1/6.67 \text{ ms} = 150 \text{ Hz}$. This is the maximum frequency of a 300 baud data stream because normally there may be several consecutive 1s and/or several consecutive 0s in a sequence, thus reducing the frequency. As mentioned earlier, the telephone network has a 300 Hz minimum frequency response, so the fundamental frequency of the 300 baud data stream will fall outside of the telephone bandwidth. This prevents sending digital data in its pure form over the phone lines.

Frequency Shift Keying (FSK) FSK is one method used to overcome the bandwidth



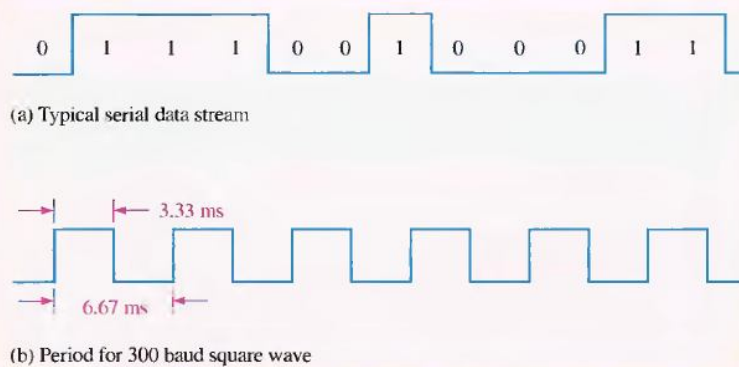
▲ FIGURE 17-52

A data communications system.



▲ **FIGURE 17-53**

Basic block diagram of a modem.



▲ **FIGURE 17-54**

A serial stream of digital data.

limitation of the telephone system so that digital data can be sent over the phone lines. The basic idea of FSK is to represent 1s and 0s by two different frequencies within the telephone bandwidth. By the way, any frequency within the telephone bandwidth is an audible tone. The standard frequen-

cies for a full-duplex 300 baud modem in the originate mode are 1070 Hz for a 0 (called a space) and 1270 Hz for a 1 (called a mark). In the answer mode, 2025 Hz is a 0 and 2225 Hz is a 1. The relationship of these FSK frequencies and the telephone bandwidth is illustrated in Figure 17-55.

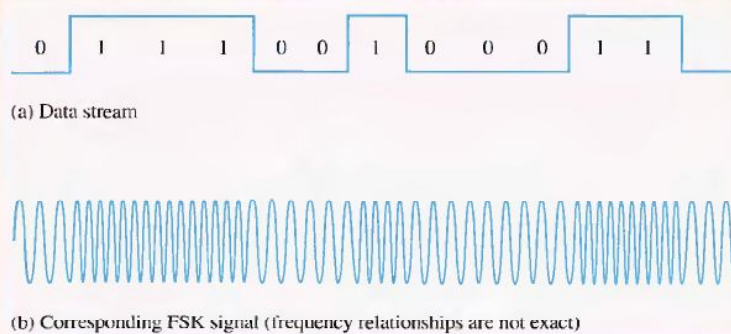
Signals in both the originate and answer bands can exist at the same time on the phone line and not interfere with each other because of the frequency separation.

An example of a digital data stream converted to FSK by a modem is shown in Figure 17-56.



▲ **FIGURE 17-55**

Frequencies for 300 baud, full-duplex data transmission.



▲ **FIGURE 17-56**

Example of FSK data.

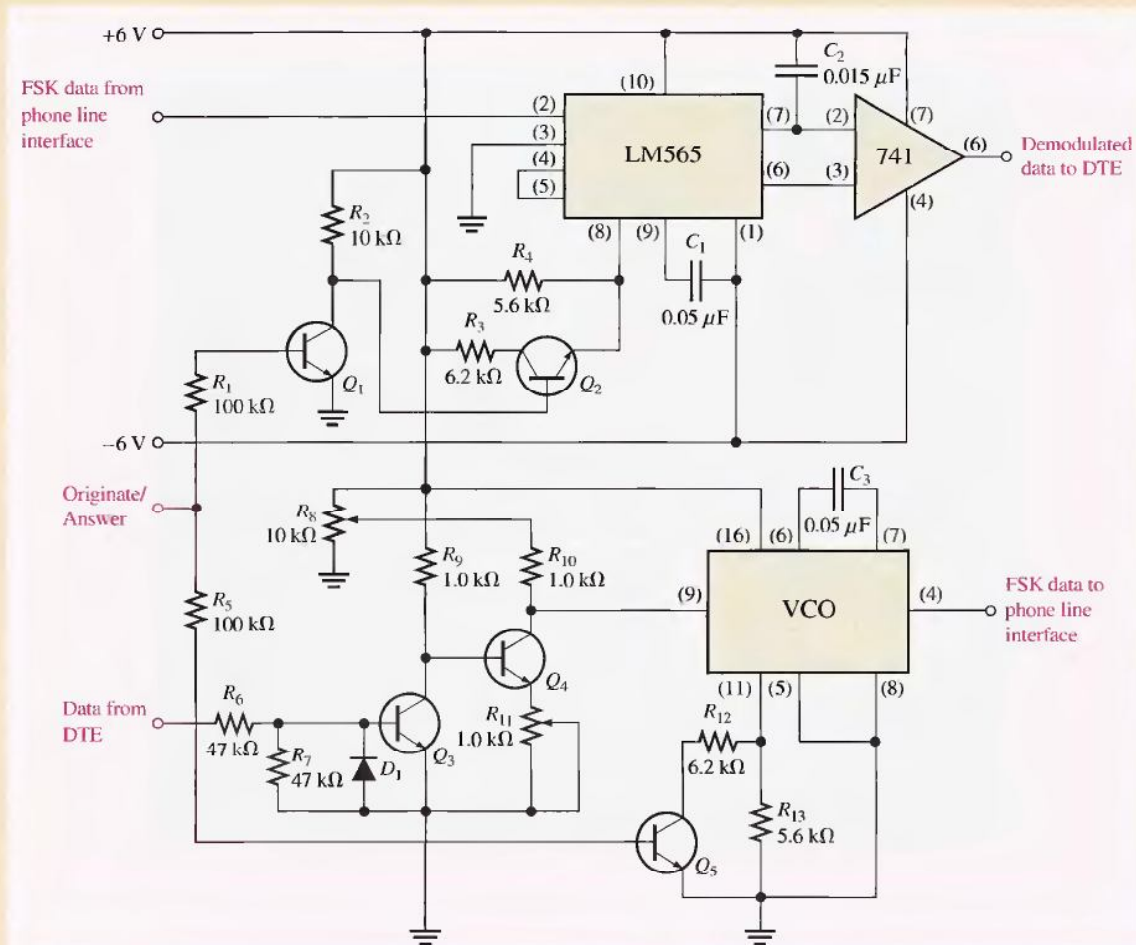
Modem Circuit Operation

The FSK modem circuits, shown in Figure 17-57, contain an LM565 PLL and a VCO integrated circuit. The VCO can be a device such as the 4046 (not covered specifically in this chapter), which is a PLL device in which the VCO portion can be used by itself because all of the necessary inputs and outputs are available. The VCO in the LM565 cannot be used indepen-

dently of the PLL because there is no input pin for the control voltage.

The function of the VCO is to accept digital data from a DTE and provide FSK modulation. The VCO is always the transmitting device. The digital data come in on the control voltage input (pin 9) of the VCO via a level-shifting circuit formed by Q_3 and Q_4 . This circuit is used because the data from the RS-232C

interface are dual polarity with a positive voltage representing a 0 and a negative voltage representing a 1. Potentiometer R_8 is for adjusting the high level of the control voltage and R_{11} is for adjusting the low level for the purpose of fine-tuning the frequency. Transistor Q_5 provides for originate/answer mode frequency selection by changing the value of the frequency-selection resis-



▲ FIGURE 17-57

FSK modulator/demodulator circuit.

tance from pin 11 to ground. Transistors Q_1 and Q_2 perform a similar function for the PLL.

When the digital data are at high levels, corresponding to logic 0s, the VCO oscillates at 1070 Hz in the originate mode and 2025 Hz in the answer mode. When the digital data are at low levels, corresponding to logic 1s, the VCO oscillates at 1270 Hz in the originate mode and 2225 Hz in the answer mode. An example of the originate mode is when a DTE issues a request for data and transmits that request to another DTE. An example of the answer mode is when the receiving

DTE responds to a request and sends data back to the originating DTE.

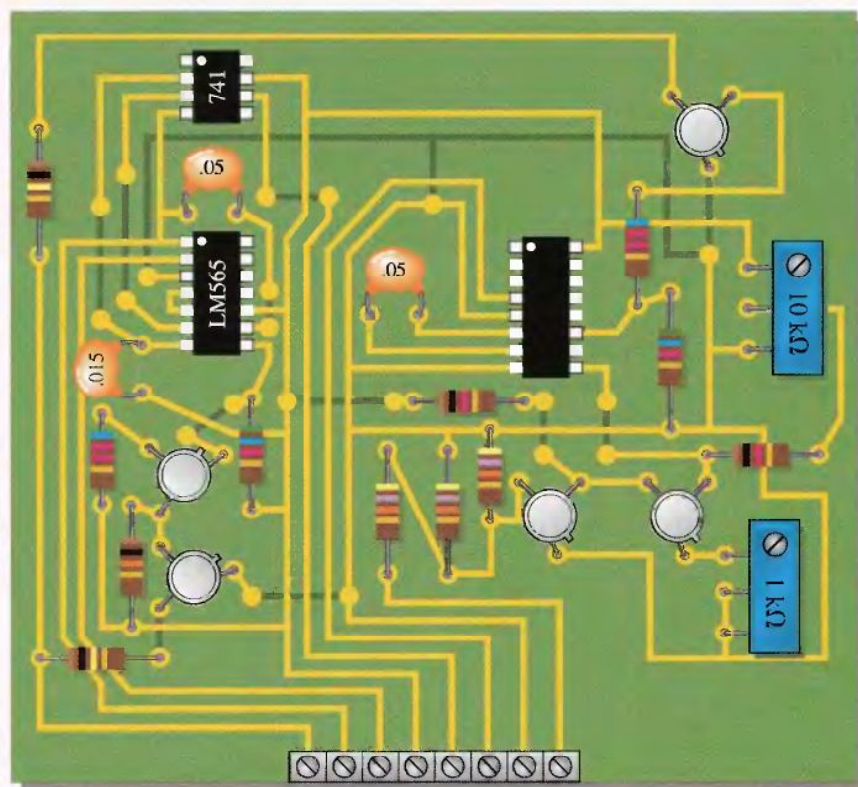
The function of the PLL is to accept incoming FSK-modulated data and convert it to a digital data format for use by the DTE. The PLL is always a receiving device. When the modem is in the originate mode, the PLL is receiving answer-mode data from the other modem. When the modem is in the answer mode, the PLL is receiving originate-mode data from the other modem. The 741 op-amp is connected as a comparator that changes the data levels from the PLL to a dual-polarity format for compatibility with the RS-232C interface.

The PC Board

Locate and identify each component and each input/output pin on the PC board in Figure 17-58 using the schematic in Figure 17-57. Verify that the board and the schematic agree. If the PC board and the schematic do not agree, indicate the problem. Backside traces are shown as darker lines.

The Circuits

For this application, the free-running frequencies of both the PLL and the VCO circuits are determined by the formula in Equation 17-5.



▲ FIGURE 17-58

- Verify that the free-running frequency for the PLL IC is approximately 1070 Hz in the originate mode and approximately 1270 Hz in the answer mode.
- Repeat the previous step for the VCO.
- Determine the approximate minimum and maximum output voltages for the 741 comparator.
- Determine the maximum high-level voltage on pin 9 of the VCO.
- If a 300 Hz square wave that varies from +5 V to -5 V is applied to the data from the DTE input, what should you observe on pin 4 of the VCO?

- When the data from the DTE are low, pin 9 of the VCO is at approximately 0 V. At this level, the VCO oscillates at 1070 Hz or 2025 Hz. When the data from the DTE go high, to what value should the voltage at pin 9 be adjusted to produce a 1270 Hz or 2225 Hz frequency if the transfer function of the VCO is 50 Hz/V?

Troubleshooting

- There is no demodulated data output voltage when there are verified FSK data from the phone line interface.
- The LM565 properly demodulates 1070 Hz and 1270 Hz FSK data but

does not properly demodulate 2025 Hz and 2225 Hz data.

- The VCO produces no FSK output.
- The VCO produces a continuous 1070 Hz tone in the originate mode and a continuous 2025 Hz tone in the answer mode when there are proper data from the DTE.

Final Report (Optional)

Describe the overall operation of the FSK modem board. Specify how each circuit works and its purpose. Identify the function of each component. Use the results previously found as appropriate.

CHAPTER SUMMARY

- In amplitude modulation (AM), the amplitude of a higher-frequency carrier signal is varied by a lower-frequency modulating signal (usually an audio signal).
- A basic superheterodyne AM receiver consists of an RF amplifier (not always), a mixer, a local oscillator, an IF (intermediate frequency) amplifier, an AM detector, and audio and power amplifiers.
- The IF in a standard AM receiver is 455 kHz.
- The AGC (automatic gain control) in a receiver tends to keep the signal strength constant within the receiver to compensate for variations in the received signal.
- In frequency modulation (FM), the frequency of a carrier signal is varied by a modulating signal.
- A superheterodyne FM receiver is basically the same as an AM receiver except that it requires a limiter to keep the IF amplitude constant, a different kind of detector or discriminator, and a deemphasis network. The IF is 10.7 MHz.
- A four-quadrant linear multiplier can handle any combination of voltage polarities on its inputs.
- Amplitude modulation is basically a multiplication process.
- The multiplication of sinusoidal signals produces sum and difference frequencies.
- The output spectrum of a balanced modulator includes upper-side and lower-side frequencies, but no carrier frequency.
- The output spectrum of a standard amplitude modulator includes upper-side and lower-side frequencies and the carrier frequency.
- A linear multiplier is used as the mixer in receiver systems.
- A mixer converts the RF signal down to the IF signal. The radio frequency varies over the AM or FM band. The intermediate frequency is constant.
- One type of AM demodulator consists of a multiplier followed by a low-pass filter.
- The audio and power amplifiers boost the output of the detector or discriminator and drive the speaker.
- A voltage-controlled oscillator (VCO) produces an output frequency that can be varied by a control voltage. Its operation is based on a variable reactance.
- A VCO is a basic frequency modulator when the modulating signal is applied to the control voltage input.
- A phase-locked loop (PLL) is a feedback circuit consisting of a phase detector, a low-pass filter, a VCO, and sometimes an amplifier.
- The purpose of a PLL is to lock onto and track incoming frequencies.
- A linear multiplier can be used as a phase detector.
- A modem is a modulator/demodulator.
- DTE stands for digital terminal equipment.
- DCE stands for digital communications equipment.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Amplitude modulation (AM) A communication method in which a lower-frequency signal modulates (varies) the amplitude of a higher-frequency signal (carrier).

Balanced modulation A form of amplitude modulation in which the carrier is suppressed; sometimes known as *suppressed-carrier modulation*.

Capture range The range of frequencies over which a PLL can acquire lock.

Four-quadrant multiplier A linear device that produces an output voltage proportional to the product of two input voltages.

Frequency modulation (FM) A communication method in which a lower-frequency intelligence-carrying signal modulates (varies) the frequency of a higher-frequency signal.

Lock range The range of frequencies over which a PLL can maintain lock.

Mixer A device for down-converting frequencies in a receiver system.

Phase-locked loop (PLL) A device for locking onto and tracking the frequency of an incoming signal.

KEY FORMULAS

17-1	$V_{\text{OUT}} = KV_X V_Y$	Multiplier output voltage
17-2	$v_1 v_2 = \frac{V_{1(p)} V_{2(p)}}{2} \cos 2\pi(f_1 - f_2)t$ $- \frac{V_{1(p)} V_{2(p)}}{2} \cos 2\pi(f_1 + f_2)t$	Sum and difference frequencies
17-3	$V_{\text{out}} = V_{c(p)}^2 \sin 2\pi f_c t$ $+ \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi(f_c - f_m)t$ $- \frac{V_{c(p)} V_{m(p)}}{2} \cos 2\pi(f_c + f_m)t$	Standard AM
17-4	$V_c = \frac{V_i V_o}{2} \cos \theta_e$	PLL control voltage
17-5	$f_o \cong \frac{1.2}{4R_1 C_1}$	Output frequency LM565
17-6	$f_{\text{lock}} = \pm \frac{8f_o}{V_{CC}}$	Lock range LM565
17-7	$f_{\text{cap}} \cong \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_{\text{lock}}}{(3600 \Omega) C_2}}$	Capture range LM565

CIRCUIT-ACTION QUIZ

Answers are at the end of the chapter.

- If R_2 in Figure 17-11 is increased in value, the output voltage of the multiplier will
(a) increase (b) decrease (c) not change
- If R_L in Figure 17-11 is decreased in value, the output voltage will
(a) increase (b) decrease (c) not change
- Refer to Figure 17-26. If the amplitude modulating frequency is increased, the lower-side frequency will
(a) increase (b) decrease (c) not change
- Refer to Figure 17-26. If the carrier frequency is decreased, the upper-side frequency will
(a) increase (b) decrease (c) not change
- In amplitude modulation, if the amplitude of the modulating signal increases, the carrier frequency will
(a) increase (b) decrease (c) not change
- If a resistor is added in series with C_4 in Figure 17-39, the voltage gain will
(a) increase (b) decrease (c) not change
- If R_1 in Figure 17-51 is increased in value, the oscillation frequency will
(a) increase (b) decrease (c) not change
- If C_1 in Figure 17-51 is decreased in value, the lock range will
(a) increase (b) decrease (c) not change

SELF-TEST

Answers are at the end of the chapter.

1. In amplitude modulation, the pattern produced by the peaks of the carrier signal is called the
(a) index (b) envelope (c) audio signal (d) upper-side frequency
2. Which of the following is not a part of an AM superheterodyne receiver?
(a) Mixer (b) IF amplifier (c) DC restorer
(d) Detector (e) Audio amplifier (f) Local oscillator
3. In an AM receiver, the local oscillator always produces a frequency that is above the incoming RF by
(a) 10.7 kHz (b) 455 MHz (c) 10.7 MHz (d) 455 kHz
4. An FM receiver has an intermediate frequency that is
(a) in the 88 MHz to 108 MHz range
(b) in the 540 kHz to 1640 kHz range
(c) 455 kHz
(d) greater than the IF in an AM receiver
5. The detector or discriminator in an AM or an FM receiver
(a) detects the difference frequency from the mixer
(b) changes the RF to IF
(c) recovers the audio signal
(d) maintains a constant IF amplitude
6. In order to handle all combinations of input voltage polarities, a multiplier must have
(a) four-quadrant capability
(b) three-quadrant capability
(c) four inputs
(d) dual-supply voltages
7. The internal attenuation of a multiplier is called the
(a) transconductance (b) scale factor (c) reduction factor
8. When the two inputs of a multiplier are connected together, the device operates as a
(a) voltage doubler (b) square root circuit
(c) squaring circuit (d) averaging circuit
9. Amplitude modulation is basically a
(a) summing of two signals (b) multiplication of two signals
(c) subtraction of two signals (d) nonlinear process
10. The frequency spectrum of a balanced modulator contains
(a) a sum frequency (b) a difference frequency (c) a carrier frequency
(d) answers (a), (b), and (c) (e) answers (a) and (b) (f) answers (b) and (c)
11. The IF in a receiver is the
(a) sum of the local oscillator frequency and the RF carrier frequency
(b) local oscillator frequency
(c) difference of the local oscillator frequency and the carrier RF frequency
(d) difference of the carrier frequency and the audio frequency
12. When a receiver is tuned from one RF frequency to another,
(a) the IF changes by an amount equal to the LO (local oscillator) frequency
(b) the IF stays the same
(c) the LO frequency changes by an amount equal to the audio frequency
(d) both the LO and the IF frequencies change
13. The output of the AM detector goes directly to the
(a) IF amplifier (b) mixer (c) audio amplifier (d) speaker

14. If the control voltage to a VCO increases, the output frequency
 - (a) decreases (b) does not change (c) increases
15. A PLL maintains lock by comparing
 - (a) the phase of two signals
 - (b) the frequency of two signals
 - (c) the amplitude of two signals

PROBLEMS

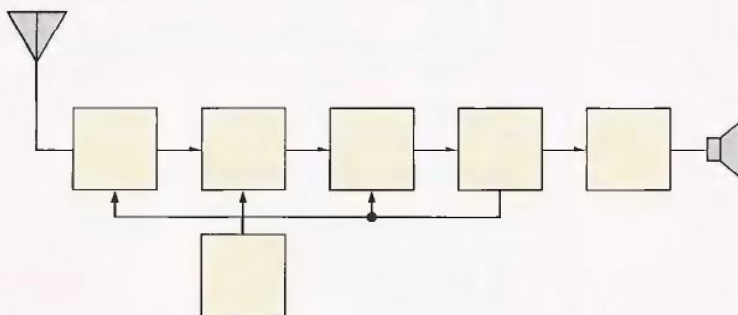
Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

SECTION 17-1 Basic Receivers

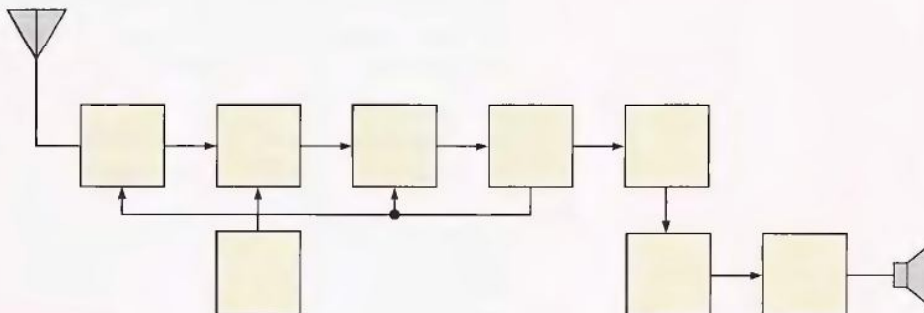
1. Label each block in the AM receiver in Figure 17-59.

► FIGURE 17-59



2. Label each block in the FM receiver in Figure 17-60.

► FIGURE 17-60

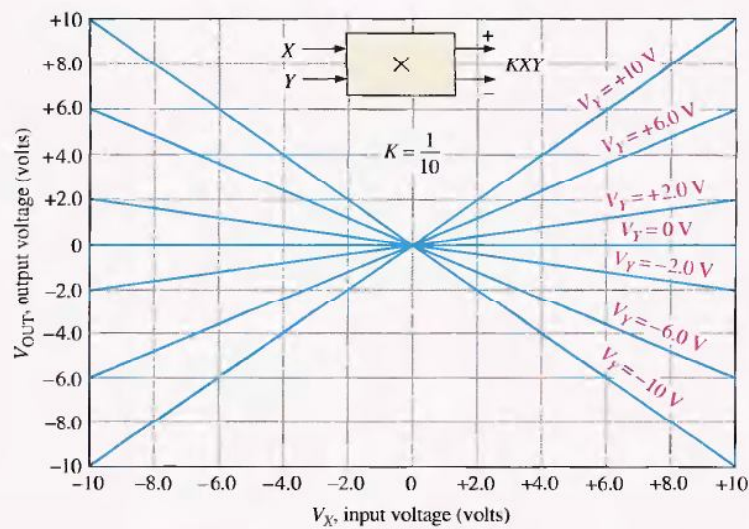


3. An AM receiver is tuned to a transmitted frequency of 680 kHz. What is the local oscillator (LO) frequency?
4. An FM receiver is tuned to a transmitted frequency of 97.2 MHz. What is the LO frequency?
5. The LO in an FM receiver is running at 101.9 MHz. What is the incoming RF? What is the IF?

SECTION 17-2 The Linear Multiplier

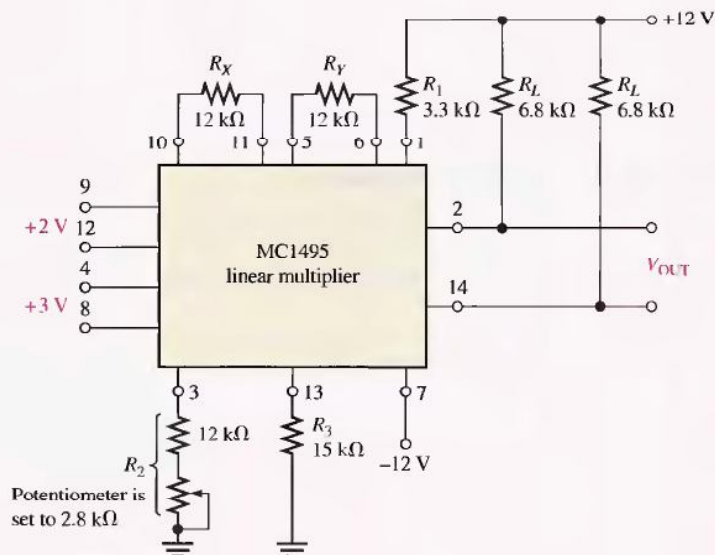
6. From the graph in Figure 17-61, determine the multiplier output voltage for each of the following pairs of input voltages.
 - (a) $V_X = -4\text{ V}$, $V_Y = +6\text{ V}$ (b) $V_X = +8\text{ V}$, $V_Y = -2\text{ V}$
 - (c) $V_X = -5\text{ V}$, $V_Y = -2\text{ V}$ (d) $V_X = +10\text{ V}$, $V_Y = +10\text{ V}$

FIGURE 17-61



7. How much pin 3 current is there for the multiplier in Figure 17-62? The potentiometer is set at $2.8\text{ k}\Omega$.
8. Determine the scale factor for the multiplier in Figure 17-62.

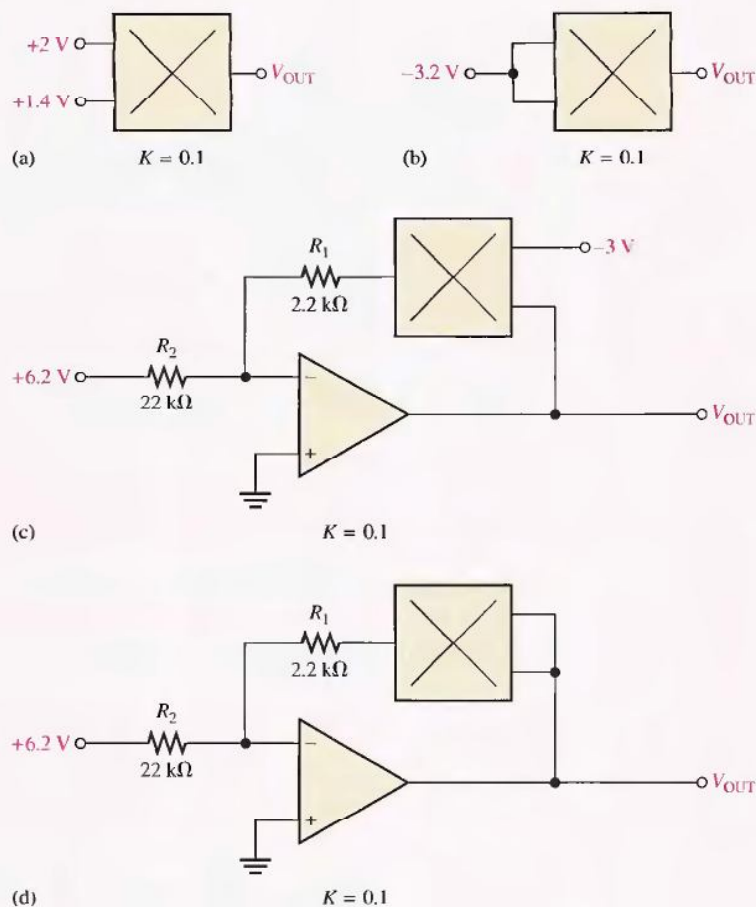
FIGURE 17-62



9. If a certain multiplier has a scale factor of 0.8 and the inputs are $+3.5\text{ V}$ and -2.9 V , what is the output voltage?
10. Show the connections for the multiplier in Figure 17-62 in order to implement a squaring circuit.

11. Determine the output voltage for each circuit in Figure 17-63.

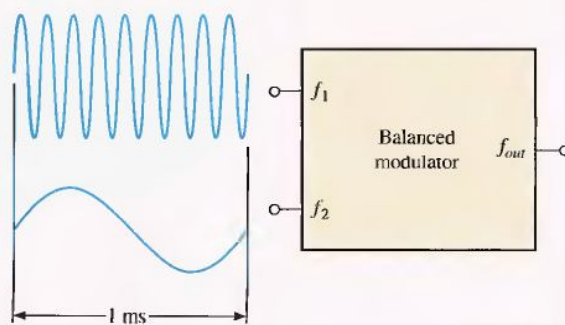
► FIGURE 17-63



SECTION 17-3 Amplitude Modulation

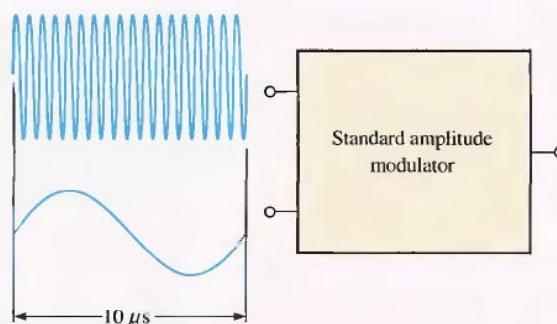
12. If a 100 kHz signal and a 30 kHz signal are applied to a balanced modulator, what frequencies will appear on the output?
13. What are the frequencies on the output of the balanced modulator in Figure 17-64?

► FIGURE 17-64



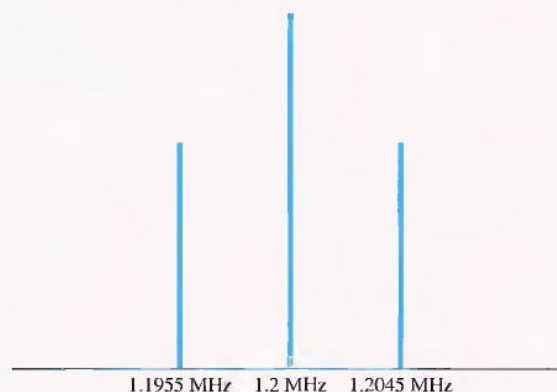
14. If a 1000 kHz signal and a 3 kHz signal are applied to a standard amplitude modulator, what frequencies will appear on the output?
15. What are the frequencies on the output of the standard amplitude modulator in Figure 17-65?

► FIGURE 17-65



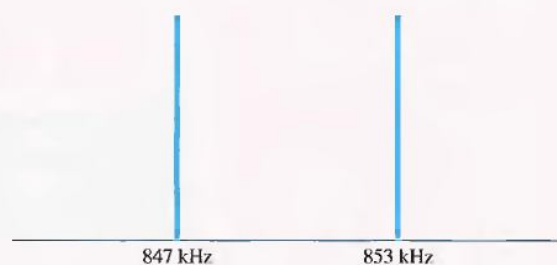
16. The frequency spectrum in Figure 17-66 is for the output of a standard amplitude modulator. Determine the carrier frequency and the modulating frequency.

► FIGURE 17-66



17. The frequency spectrum in Figure 17-67 is for the output of a balanced modulator. Determine the carrier frequency and the modulating frequency.

► FIGURE 17-67

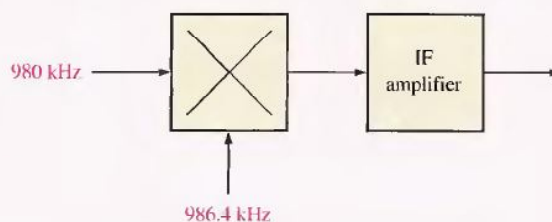


18. A voice signal ranging from 300 Hz to 3 kHz amplitude modulates a 600 kHz carrier. Develop the frequency spectrum.

SECTION 17-4 The Mixer

19. Determine the output expression for a multiplier with one sinusoidal input having a peak voltage of 0.2 V and a frequency of 2200 kHz and the other input having a peak voltage of 0.15 V and a frequency of 3300 kHz.
20. Determine the output frequency of the IF amplifier for the frequencies shown in Figure 17-68.

► FIGURE 17-68

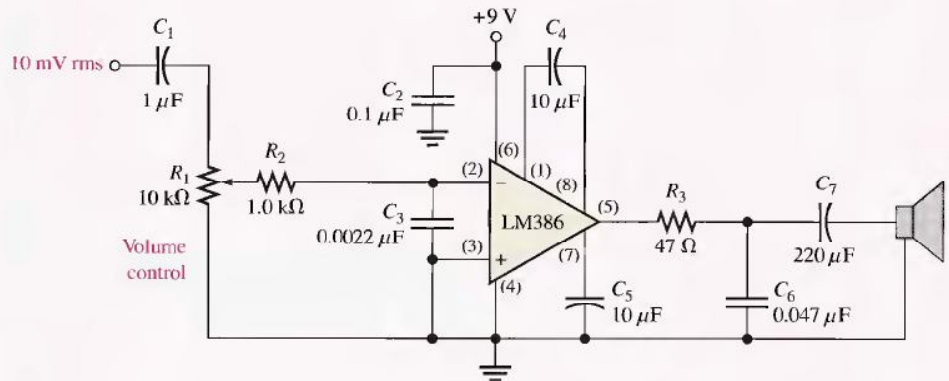


SECTION 17-5 AM Demodulation

21. The input to a certain AM receiver consists of a 1500 kHz carrier and two side frequencies separated from the carrier by 20 kHz. Determine the frequency spectrum at the output of the mixer amplifier.
22. For the same conditions stated in Problem 21, determine the frequency spectrum at the output of the IF amplifier.
23. For the same conditions stated in Problem 21, determine the frequency spectrum at the output of the AM detector (demodulator).

SECTION 17-6 IF and Audio Amplifiers

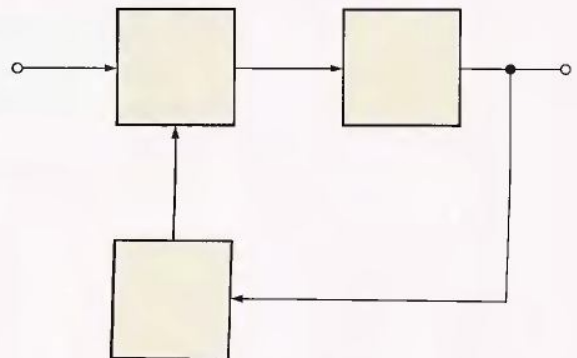
24. For a carrier frequency of 1.2 MHz and a modulating frequency of 8.5 kHz, list all of the frequencies on the output of the mixer in an AM receiver.
25. In a certain AM receiver, one amplifier has a passband from 450 kHz to 460 kHz and another has a passband from 10 Hz to 5 kHz. Identify these amplifiers.
26. Determine the maximum and minimum output voltages for the audio power amplifier in Figure 17-69.

FIGURE 17-69**SECTION 17-7 Frequency Modulation**

27. Explain how a VCO is used as a frequency modulator.
28. How does an FM signal differ from an AM signal?
29. What is the variable reactance element shown in Figure 17-42?

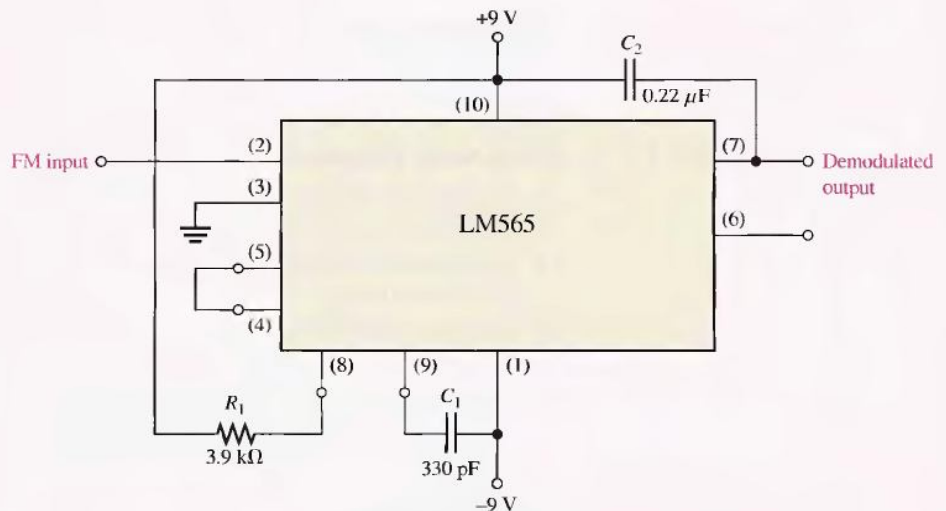
SECTION 17-8 The Phase-Locked Loop (PLL)

30. Label each block in the PLL diagram of Figure 17-70.

FIGURE 17-70

31. A PLL is locked onto an incoming signal with a peak amplitude of 250 mV and a frequency of 10 MHz at a phase angle of 30° . The 400 mV peak VCO signal is at a phase angle of 15° .
 - (a) What is the VCO frequency?
 - (b) What is the value of the control voltage being fed back to the VCO at this point?
32. What is the conversion gain of a VCO if a 0.5 V increase in the control voltage causes the output frequency to increase by 3.6 kHz?
33. If the conversion gain of a certain VCO is 1.5 kHz per volt, how much does the frequency change if the control voltage increases 0.67 V?
34. Name two conditions for a PLL to acquire lock.
35. Determine the free-running frequency, the lock range, and the capture range for the PLL in Figure 17-71.

FIGURE 17-71



ANSWERS

SECTION REVIEWS

SECTION 17-1 Basic Receivers

1. AM is amplitude modulation. FM is frequency modulation.
2. In AM, the modulating signal varies the amplitude of a carrier. In FM, the modulating signal varies the frequency of a carrier.
3. AM: 540 kHz to 1640 kHz; FM: 88 MHz to 108 MHz

SECTION 17-2 The Linear Multiplier

1. A four-quadrant multiplier can handle any combination (4) of positive and negative inputs. A one-quadrant multiplier can only handle two positive inputs, for example.
2. $K = 0.1$. K must be 1 for an output of 5 V.
3. Connect the two inputs together and apply a single input variable.

SECTION 17-3 Amplitude Modulation

1. Amplitude modulation is the process of varying the amplitude of a carrier signal with a modulating signal.
2. Balanced modulation produces no carrier frequency on the output, whereas standard AM does.
3. The carrier signal is the modulated signal and has a sufficiently high frequency for transmission. The modulating signal is a lower-frequency signal that contains information and varies the carrier amplitude according to its waveshape.

4. The upper-side frequency is the sum of the carrier frequency and the modulating frequency. The lower-side frequency is the difference of the carrier frequency and the modulating frequency.
5. By summing the peak carrier voltage and the modulating signal before mixing with the carrier signal

SECTION 17-4 The Mixer

1. The mixer produces (among other frequencies) a signal representing the difference between the incoming carrier frequency and the local oscillator frequency. This is called the intermediate frequency.
2. The mixer multiplies the carrier and the local oscillator signals.
3. $1000 \text{ kHz} + 350 \text{ kHz} = 1350 \text{ kHz}$, $1000 \text{ kHz} - 350 \text{ kHz} = 650 \text{ kHz}$

SECTION 17-5 AM Demodulation

1. The filter removes all frequencies except the audio.
2. Only the 1 kHz

SECTION 17-6 IF and Audio Amplifiers

1. To amplify the 455 kHz amplitude modulated IF coming from the mixer
2. The IF center frequency is 455 kHz.
3. The 10 kHz bandwidth allows the upper-side and lower-side frequencies that contain the information to pass.
4. The audio amplifier follows the detector because the detector is the circuit that recovers the audio from the modulated IF.
5. The IF has a response of approximately $455 \text{ kHz} \pm 5 \text{ kHz}$. The typical audio amplifier has a maximum bandwidth from tens of hertz up to about 15 kHz although for many amplifiers, the bandwidth can be much less than this typical maximum.

SECTION 17-7 Frequency Modulation

1. The frequency variation of an FM signal bears the information.
2. VCOs are based on the principle of voltage-variable reactance.

SECTION 17-8 The Phase-Locked Loop (PLL)

1. Phase detector, low-pass filter, and VCO
2. Sometimes a PLL uses an amplifier in the loop.
3. A PLL locks onto and tracks a variable incoming frequency.
4. The lock range specifies how much a lock-on frequency can deviate without the PLL losing lock. The capture range specifies how close the incoming frequency must be from the free-running VCO frequency in order for the PLL to lock.
5. The PLL detects a change in the phase of the incoming signal compared to the VCO signal that indicates a change in frequency. The positive feedback then causes the VCO frequency to change along with the incoming frequency.

RELATED PROBLEMS FOR EXAMPLES

- 17-1 -3.6 V from the graph in Figure 17-9
- 17-2 0.728 V
- 17-3 Modulate the carrier with a higher-frequency signal.
- 17-4 The balanced modulator output has the same side frequencies but does not have a carrier frequency.
- 17-5 $V_p = 0.025 \text{ mV}$, $f = 455 \text{ kHz}$

17-6 455 kHz

17-7 0.172 V

17-8 A decrease of 6 kHz; 244 kHz

17-9 Decrease C_2 to 0.0595 μF .

CIRCUIT-ACTION QUIZ

1. (a) 2. (b) 3. (b) 4. (b) 5. (c) 6. (b) 7. (b) 8. (a)

SELF-TEST

1. (b) 2. (c) 3. (d) 4. (d) 5. (c) 6. (a) 7. (b) 8. (c)
9. (b) 10. (e) 11. (c) 12. (b) 13. (c) 14. (c) 15. (a)

18

VOLTAGE REGULATORS

INTRODUCTION

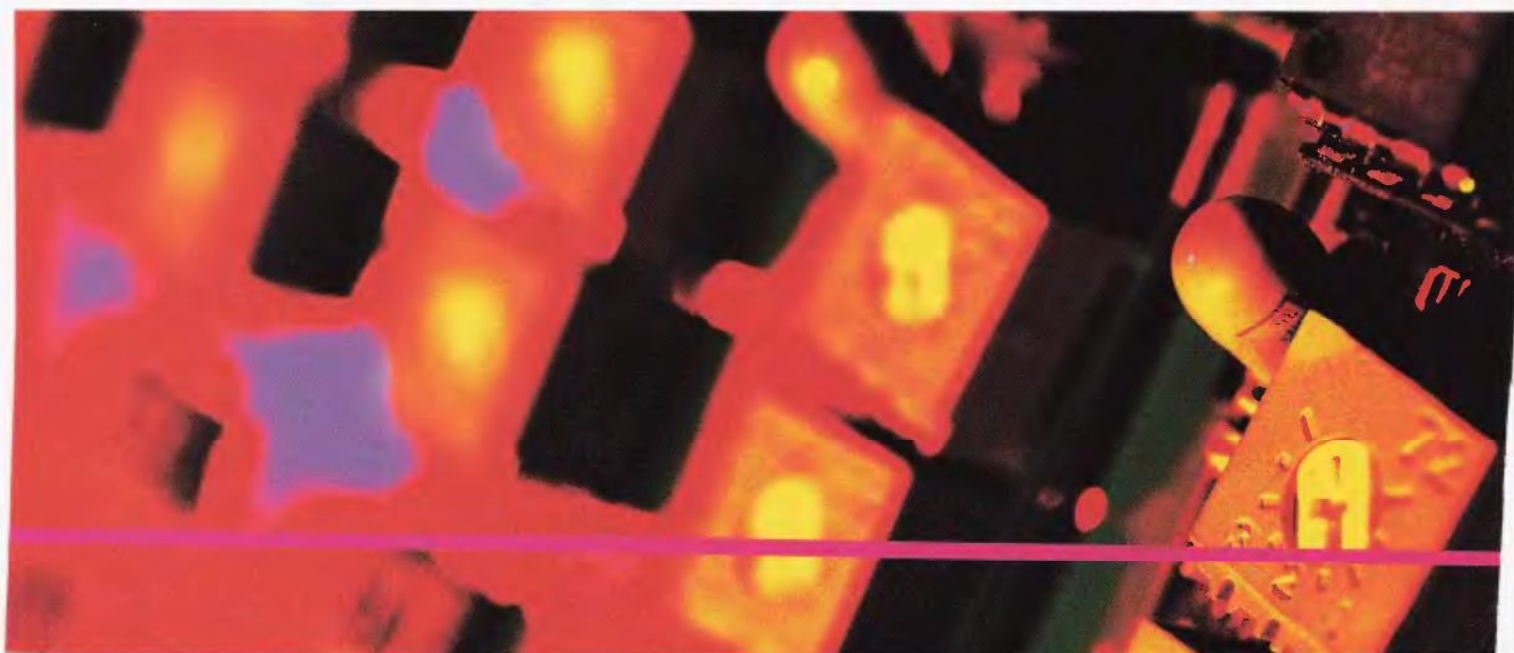
A voltage regulator provides a constant dc output voltage that is essentially independent of the input voltage, output load current, and temperature. The voltage regulator is one part of a power supply. Its input voltage comes from the filtered output of a rectifier derived from an ac voltage or from a battery in the case of portable systems.

Most voltage regulators fall into two broad categories: linear regulators and switching regulators. In the linear regulator category, two general types are the series regulator and the shunt regulator. These are normally available for either positive or negative output voltages. A dual regulator provides both positive and negative outputs. In the switching regulator category, three general configurations are step-down, step-up, and inverting.

Many types of integrated circuit (IC) regulators are available. The most popular types of linear regulator are the three-terminal fixed voltage regulator and the three-terminal adjustable voltage regulator. Switching regulators are also widely used. In this chapter, specific IC devices are introduced as representative of the wide range of available devices.

CHAPTER OUTLINE

- 18-1 Voltage Regulation
- 18-2 Basic Series Regulators
- 18-3 Basic Shunt Regulators
- 18-4 Basic Switching Regulators
- 18-5 Integrated Circuit Voltage Regulators
- 18-6 Applications of IC Voltage Regulators
- ■ ■ System Application



CHAPTER OBJECTIVES

- Describe the basic concept of voltage regulation
- Discuss the principles of series voltage regulators
- Discuss the principles of shunt voltage regulators
- Discuss the principles of switching regulators
- Discuss integrated circuit voltage regulators
- Discuss applications of IC voltage regulators

KEY TERMS

- Regulator
- Line regulation
- Load regulation
- Linear regulator
- Switching regulator
- Thermal overload

SYSTEM APPLICATION PREVIEW

A dual-polarity power supply is to be used for the FM receiver from Chapter 15. Two regulators, one positive and the other negative, provide the positive voltage required for the receiver circuits and the dual-polarity voltages for the op-amp circuits.

WWW. VISIT THE COMPANION WEBSITE

Study aids for this chapter are available at
<http://www.prenhall.com/floyd>

18-1 VOLTAGE REGULATION

Two basic categories of voltage regulation are line regulation and load regulation. The purpose of line regulation is to maintain a nearly constant output voltage when the input voltage varies. The purpose of load regulation is to maintain a nearly constant output voltage when the load varies.

After completing this section, you should be able to

- Describe the basic concept of voltage regulation
- Explain line regulation
- Calculate line regulation
- Explain load regulation
- Calculate load regulation

Line Regulation



When the dc input (line) voltage changes, an electronic circuit called a **regulator** maintains a nearly constant output voltage, as illustrated in Figure 18-1. **Line regulation** can be defined as the percentage change in the output voltage for a given change in the input (line) voltage. When taken over a range of input voltage values, line regulation is expressed as a percentage by the following formula:

Equation 18-1

$$\text{Line regulation} = \left(\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right) 100\%$$

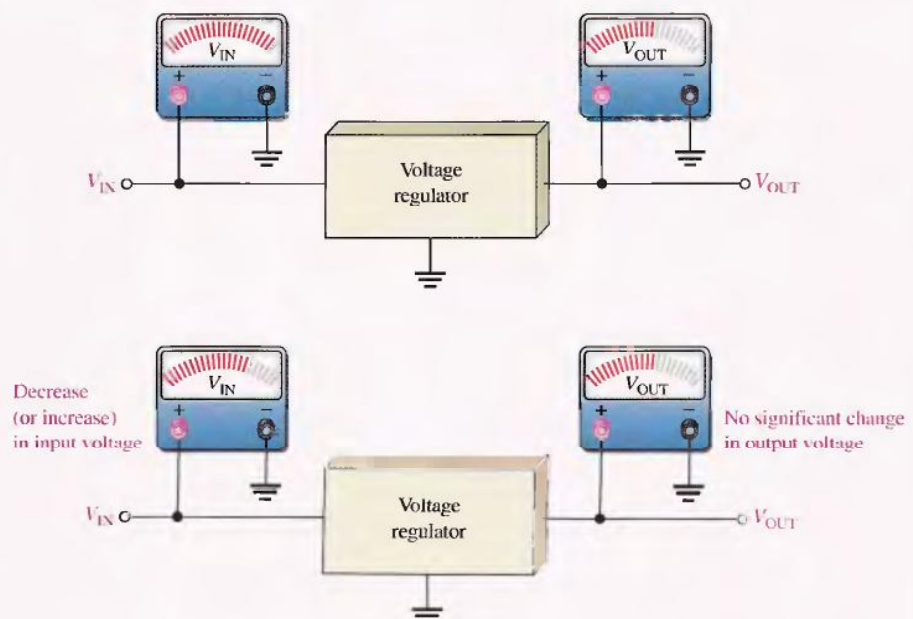
Line regulation can also be expressed in units of %/V. For example, a line regulation of 0.05%/V means that the output voltage changes 0.05 percent when the input voltage increases or decreases by one volt. Line regulation can be calculated using the following formula (Δ means “a change in”):

Equation 18-2

$$\text{Line regulation} = \frac{(\Delta V_{\text{OUT}} / V_{\text{OUT}}) 100\%}{\Delta V_{\text{IN}}}$$

► FIGURE 18-1

Line regulation. A change in input (line) voltage does not significantly affect the output voltage of a regulator (within certain limits).



EXAMPLE 18-1

When the input to a particular voltage regulator decreases by 5 V, the output decreases by 0.25 V. The nominal output is 15 V. Determine the line regulation in %/V.

Solution The line regulation as a percentage change per volt is

$$\text{line regulation} = \frac{(\Delta V_{\text{OUT}}/V_{\text{OUT}})100\%}{\Delta V_{\text{IN}}} = \frac{(0.25 \text{ V}/15 \text{ V})100\%}{5 \text{ V}} = 0.333\%/\text{V}$$

Related Problem * The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.42 V. The nominal output is 20 V. Determine the regulation in %/V.

*Answers are at the end of the chapter.

Load Regulation

When the amount of current through a load changes due to a varying load resistance, the voltage regulator must maintain a nearly constant output voltage across the load, as illustrated in Figure 18-2.

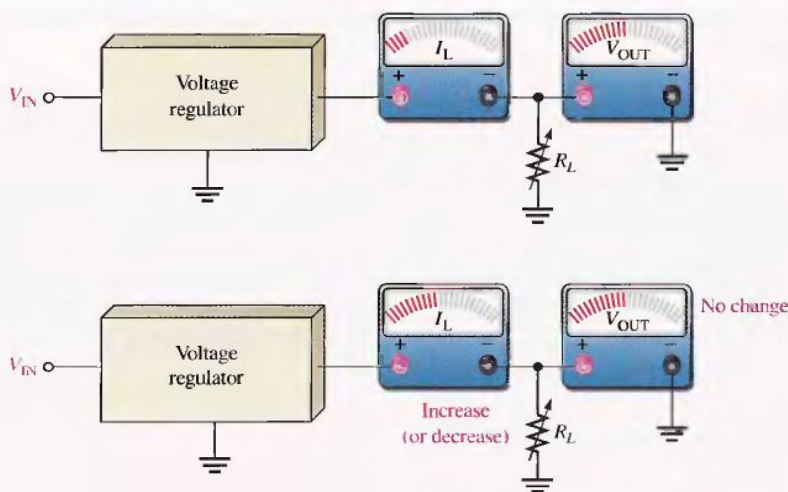


FIGURE 18-2

Load regulation. A change in load current has practically no effect on the output voltage of a regulator (within certain limits).

Load regulation can be defined as the percentage change in output voltage for a given change in load current. One way to express load regulation is as a percentage change in output voltage from no-load (NL) to full-load (FL).

$$\text{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \right) 100\%$$

Equation 18-3

Alternately, the load regulation can be expressed as a percentage change in output voltage for each mA change in load current. For example, a load regulation of 0.01%/mA means that the output voltage changes 0.01 percent when the load current increases or decreases 1 mA.

EXAMPLE 18-2

A certain voltage regulator has a 12 V output when there is no load ($I_L = 0$). When there is a full-load current of 10 mA, the output voltage is 11.9 V. Express the voltage regulation as a percentage change from no-load to full-load and also as a percentage change for each mA change in load current.

Solution The no-load output voltage is

$$V_{NL} = 12 \text{ V}$$

The full-load output voltage is

$$V_{FL} = 11.9 \text{ V}$$

The load regulation as a percentage change from no-load to full-load is

$$\text{load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) 100\% = \left(\frac{12 \text{ V} - 11.9 \text{ V}}{11.9 \text{ V}} \right) 100\% = \mathbf{0.840\%}$$

The load regulation can also be expressed as a percentage change per milliamp as

$$\text{load regulation} = \frac{0.840\%}{10 \text{ mA}} = \mathbf{0.084\%/mA}$$

where the change in load current from no-load to full-load is 10 mA.

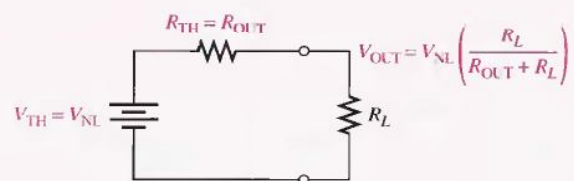
Related Problem A regulator has a no-load output voltage of 18 V and a full-load output of 17.8 V at a load current of 50 mA. Determine the voltage regulation as a percentage change from no-load to full-load and also as a percentage change for each mA change in load current.

Sometimes power supply manufacturers specify the equivalent output resistance of a power supply (R_{OUT}) instead of its load regulation. Recall that an equivalent Thevenin circuit can be drawn for any two-terminal linear circuit. Figure 18-3 shows the equivalent Thevenin circuit for a power supply with a load resistor. The Thevenin voltage is the voltage from the supply with no load (V_{NL}), and the Thevenin resistance is the specified output resistance, R_{OUT} . Ideally, R_{OUT} is zero, corresponding to 0% load regulation, but in practical power supplies R_{OUT} is a small value. With the load resistor in place, the output voltage is found by applying the voltage-divider rule:

$$V_{OUT} = V_{NL} \left(\frac{R_L}{R_{OUT} + R_L} \right)$$

FIGURE 18-3

Thevenin equivalent circuit for a power supply with a load resistor.



If we let R_{FL} equal the smallest-rated load resistance (largest-rated current), then the full-load output voltage (V_{FL}) is

$$V_{FL} = V_{NL} \left(\frac{R_{FL}}{R_{OUT} + R_{FL}} \right)$$

By rearranging and substituting into Equation 18-3,

$$V_{NL} = V_{FL} \left(\frac{R_{OUT} + R_{FL}}{R_{FL}} \right)$$

$$\text{Load regulation} = \frac{V_{FL} \left(\frac{R_{OUT} + R_{FL}}{R_{FL}} \right) - V_{FL}}{V_{FL}} \times 100\%$$

$$= \left(\frac{R_{OUT} + R_{FL}}{R_{FL}} - 1 \right) 100\%$$

$$\text{Load regulation} = \left(\frac{R_{OUT}}{R_{FL}} \right) 100\%$$

Equation 18-4

Equation 18-4 is a useful way of finding the percent load regulation when the output resistance and minimum load resistance are specified.

SECTION 18-1 REVIEW

Answers are at the end of the chapter.

1. Define *line regulation*.
2. Define *load regulation*.
3. The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.042 V. The nominal output is 20 V. Determine the line regulation in both % and in %/V.
4. If a 5.0 V power supply has an output resistance of 80 mΩ and a specified maximum output current of 1.0 A, what is the load regulation? Give the result as a % and as a %/mA.

18-2 BASIC SERIES REGULATORS

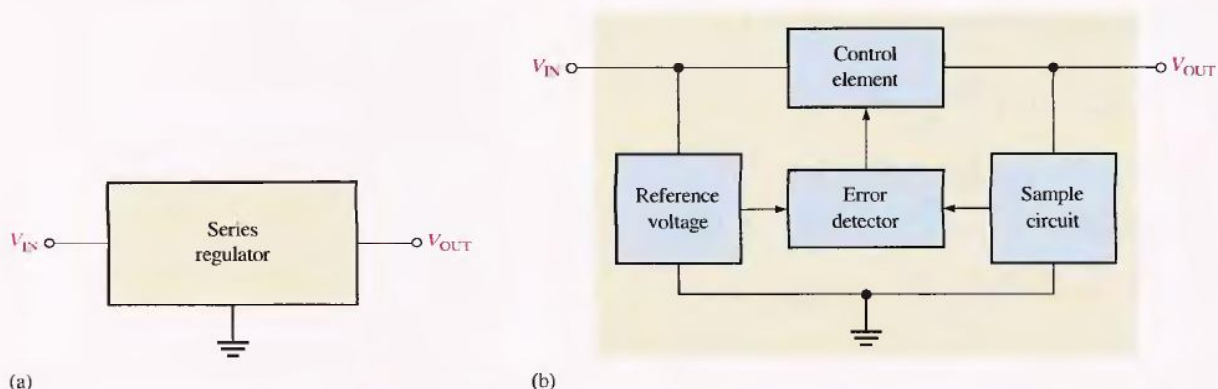
The fundamental classes of voltage regulators are linear regulators and switching regulators. Both of these are available in integrated circuit form. There are two basic types of linear regulator. One is the series regulator and the other is the shunt regulator. In this section, we will look at the series regulator. The shunt and switching regulators are covered in the next two sections.

After completing this section, you should be able to

- Discuss the principles of series voltage regulators
- Explain regulating action
- Calculate output voltage of an op-amp series regulator
- Discuss overload protection and explain how to use current limiting
- Describe a regulator with fold-back current limiting

A simple representation of a series type of **linear regulator** is shown in Figure 18-4(a), and the basic components are shown in the block diagram in Figure 18-4(b). The control element is a pass transistor in series with the load between the input and output. The output sample circuit senses a change in the output voltage. The error detector compares the





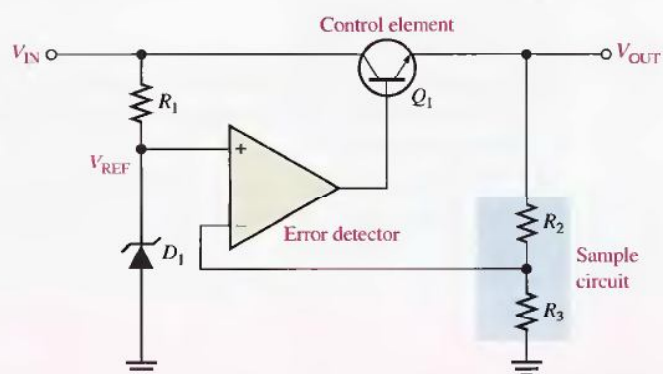
▲ FIGURE 18-4

Simple series voltage regulator and block diagram.

sample voltage with a reference voltage and causes the control element to compensate in order to maintain a constant output voltage. A basic op-amp series regulator is shown in Figure 18-5.

► FIGURE 18-5

Basic op-amp series regulator.

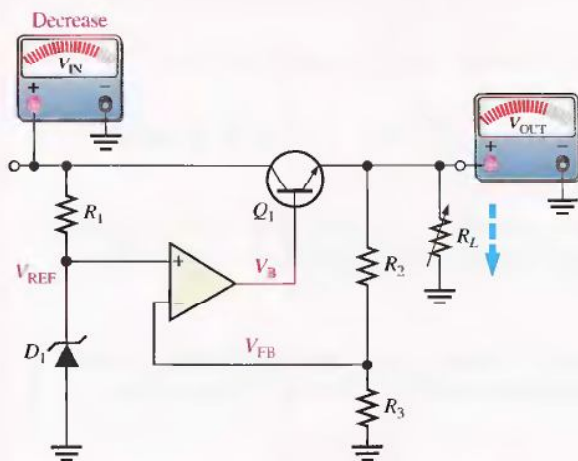


Regulating Action

The operation of the series regulator is illustrated in Figure 18-6 and is as follows. The resistive voltage divider formed by R_2 and R_3 senses any change in the output voltage. When the output tries to decrease, as indicated in Figure 18-6(a), because of a decrease in V_{IN} or because of an increase in I_L caused by a decrease in R_L , a proportional voltage decrease is applied to the op-amp's inverting input by the voltage divider. Since the zener diode (D_1) holds the other op-amp input at a nearly constant reference voltage, V_{REF} , a small difference voltage (error voltage) is developed across the op-amp's inputs. This difference voltage is amplified, and the op-amp's output voltage, V_B , increases. This increase is applied to the base of Q_1 , causing the emitter voltage V_{OUT} to increase until the voltage to the inverting input again equals the reference (zener) voltage. This action offsets the attempted decrease in output voltage, thus keeping it nearly constant. The power transistor, Q_1 , is usually used with a heat sink because it must handle all of the load current.

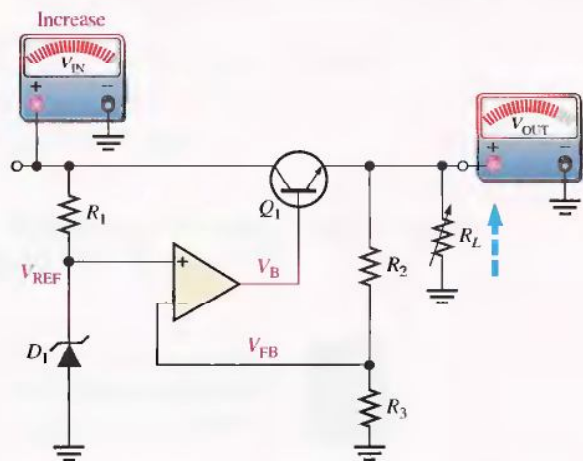
The opposite action occurs when the output tries to increase, as indicated in Figure 18-6(b). The op-amp in the series regulator is actually connected as a noninverting amplifier where the reference voltage V_{REF} is the input at the noninverting terminal, and the R_2/R_3 voltage divider forms the negative feedback circuit. The closed-loop voltage gain is

$$A_{cl} = 1 + \frac{R_2}{R_3}$$



(a) When V_{IN} or R_L decreases, V_{OUT} attempts to decrease. The feedback voltage, V_{FB} , also attempts to decrease, and as a result, the op-amp's output voltage V_B attempts to increase, thus compensating for the attempted decrease in V_{OUT} by increasing the Q_1 emitter voltage. Changes in V_{OUT} are exaggerated for illustration.

When V_{IN} (or R_L) stabilizes at its new lower value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.



(b) When V_{IN} or R_L increases, V_{OUT} attempts to increase. The feedback voltage, V_{FB} , also attempts to increase, and as a result, V_B , applied to the base of the control transistor, attempts to decrease, thus compensating for the attempted increase in V_{OUT} by decreasing the Q_1 emitter voltage.

When V_{IN} (or R_L) stabilizes at its new higher value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.

FIGURE 18-6

Illustration of series regulator action that keeps V_{OUT} constant when V_{IN} or R_L changes.

Therefore, the regulated output voltage of the series regulator (neglecting the base-emitter voltage of Q_1) is

$$V_{OUT} \cong \left(1 + \frac{R_2}{R_3}\right) V_{REF}$$

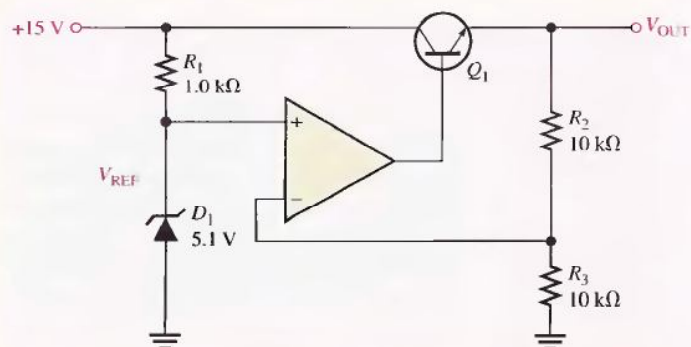
Equation 18-5

From this analysis, you can see that the output voltage is determined by the zener voltage and the resistors R_2 and R_3 . It is relatively independent of the input voltage, and therefore, regulation is achieved (as long as the input voltage and load current are within specified limits).

EXAMPLE 18-3

Determine the output voltage for the regulator in Figure 18-7.

FIGURE 18-7



Solution $V_{\text{REF}} = 5.1 \text{ V}$, the zener voltage. The regulated output voltage is therefore

$$V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3}\right)V_{\text{REF}} = \left(1 + \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega}\right)5.1 \text{ V} = (2)5.1 \text{ V} = 10.2 \text{ V}$$

Related Problem The following changes are made in the circuit in Figure 18-7: A 3.3 V zener replaces the 5.1 V zener, $R_1 = 1.8 \text{ k}\Omega$, $R_2 = 22 \text{ k}\Omega$, and $R_3 = 18 \text{ k}\Omega$. What is the output voltage?



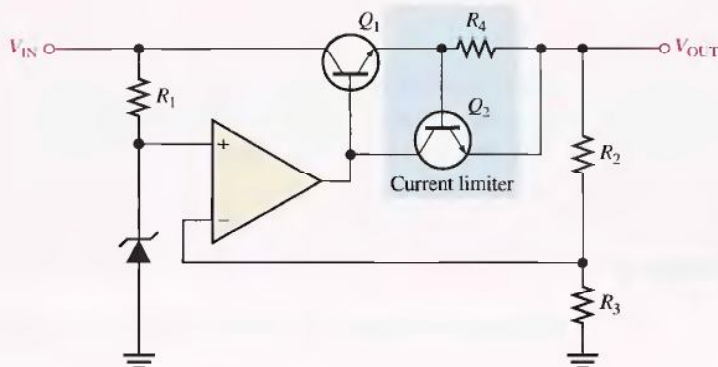
Open the Multisim file E18-03 in the Examples folder on your CD-ROM. Measure the output voltage with 15 V dc applied to the input. Compare to the calculated value.

Short-Circuit or Overload Protection

If an excessive amount of load current is drawn, the series-pass transistor can be quickly damaged or destroyed. Most regulators use some type of excess current protection in the form of a current-limiting mechanism. Figure 18-8 shows one method of current limiting to prevent overloads called *constant-current limiting*. The current-limiting circuit consists of transistor Q_2 and resistor R_4 .

► **FIGURE 18-8**

Series regulator with constant-current limiting.



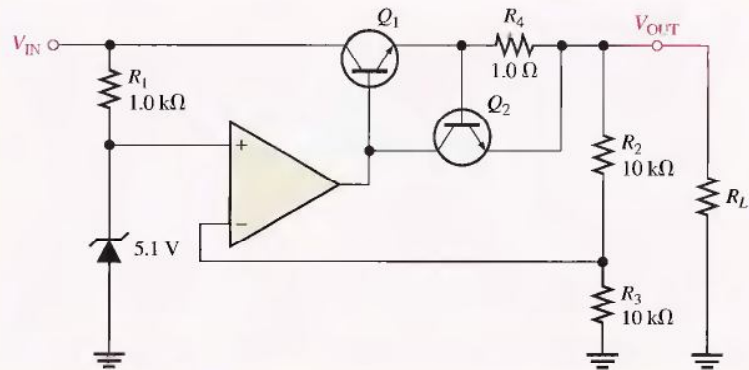
The load current through R_4 produces a voltage from base to emitter of Q_2 . When I_L reaches a predetermined maximum value, the voltage drop across R_4 is sufficient to forward-bias the base-emitter junction of Q_2 , thus causing it to conduct. Enough op-amp output current is diverted through Q_2 to reduce the Q_1 base current, so that I_L is limited to its maximum value, $I_{L(\text{max})}$. Since the base-to-emitter voltage of Q_2 cannot exceed approximately 0.7 V for a silicon transistor, the voltage across R_4 is held to this value, and the load current is limited to

Equation 18-6

$$I_{L(\text{max})} = \frac{0.7 \text{ V}}{R_4}$$

EXAMPLE 18-4

Determine the maximum current that the regulator in Figure 18-9 can provide to a load.

FIGURE 18-9**Solution**

$$I_{L(\max)} = \frac{0.7 \text{ V}}{R_4} = \frac{0.7 \text{ V}}{1.0 \Omega} = 0.7 \text{ A}$$

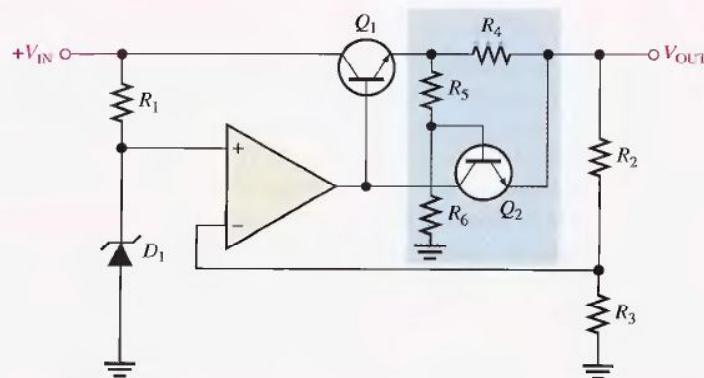
Related Problem If the output of the regulator in Figure 18-9 is shorted, what is the current?

Regulator with Fold-Back Current Limiting

In the previous current-limiting technique, the current is restricted to a maximum constant value. **Fold-back current limiting** is a method used particularly in high-current regulators whereby the output current under overload conditions drops to a value well below the peak load current capability to prevent excessive power dissipation.

The basic concept of fold-back current limiting is as follows, with reference to Figure 18-10. The circuit in the blue-shaded area is similar to the constant current-limiting arrangement in Figure 18-8, with the exception of resistors R_5 and R_6 . The voltage drop developed across R_4 by the load current must not only overcome the base-emitter voltage required to turn on Q_2 , but it must also overcome the voltage across R_5 . That is, the voltage across R_4 must be

$$V_{R4} = V_{R5} + V_{BE}$$

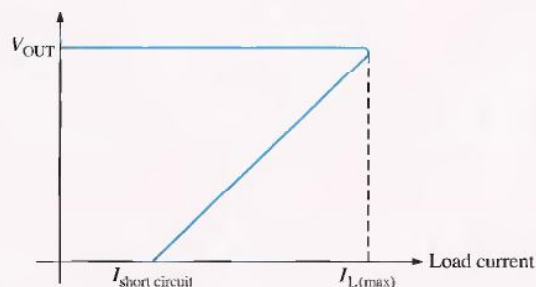
**FIGURE 18-10**

Series regulator with fold-back current limiting.

In an overload or short-circuit condition, the load current increases to a value, $I_{L(\max)}$, that is sufficient to cause Q_2 to conduct. At this point the current can increase no further. The decrease in output voltage results in a proportional decrease in the voltage across R_5 ; thus, less current through R_4 is required to maintain the forward-biased condition of Q_1 . So, as V_{OUT} decreases, I_L decreases, as shown in the graph of Figure 18-11.

► **FIGURE 18-11**

Fold-back current limiting (output voltage versus load current).



The advantage of this technique is that the regulator is allowed to operate with peak load current up to $I_{L(\max)}$; but when the output becomes shorted, the current drops to a lower value to prevent overheating of the device.

SECTION 18-2 REVIEW

1. What are the basic components in a series regulator?
2. A certain series regulator has an output voltage of 8 V. If the op-amp's closed loop gain is 4, what is the value of the reference voltage?

18-3 BASIC SHUNT REGULATORS

The second basic type of linear voltage regulator is the shunt regulator. As you have learned, the control element in the series regulator is the series pass transistor. In the shunt regulator, the control element is a transistor in parallel (shunt) with the load.

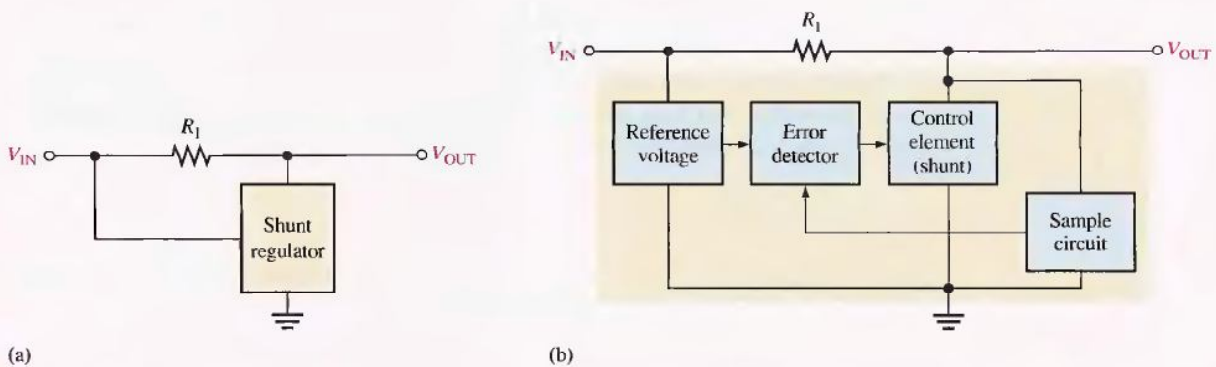
After completing this section, you should be able to

- Discuss the principles of shunt voltage regulators
- Describe the operation of a basic op-amp shunt regulator
- Compare series and shunt regulators

A simple representation of a shunt type of linear regulator is shown in Figure 18-12(a), and the basic components are shown in the block diagram in part (b).

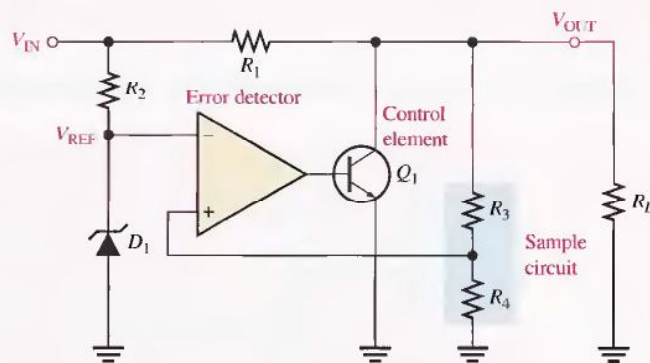
In the basic shunt regulator, the control element is a transistor, Q_1 , in parallel with the load, as shown in Figure 18-13. A resistor, R_1 , is in series with the load. The operation of the circuit is similar to that of the series regulator, except that regulation is achieved by controlling the current through the parallel transistor Q_1 .

When the output voltage tries to decrease due to a change in input voltage or load current caused by a change in load resistance, as shown in Figure 18-14(a), the attempted decrease is sensed by R_3 and R_4 and applied to the op-amp's noninverting input. The resulting difference voltage reduces the op-amp's output (V_B), driving Q_1 less, thus reducing its collector current (shunt current) and increasing its effective collector-to-emitter resistance, r'_{CE} .



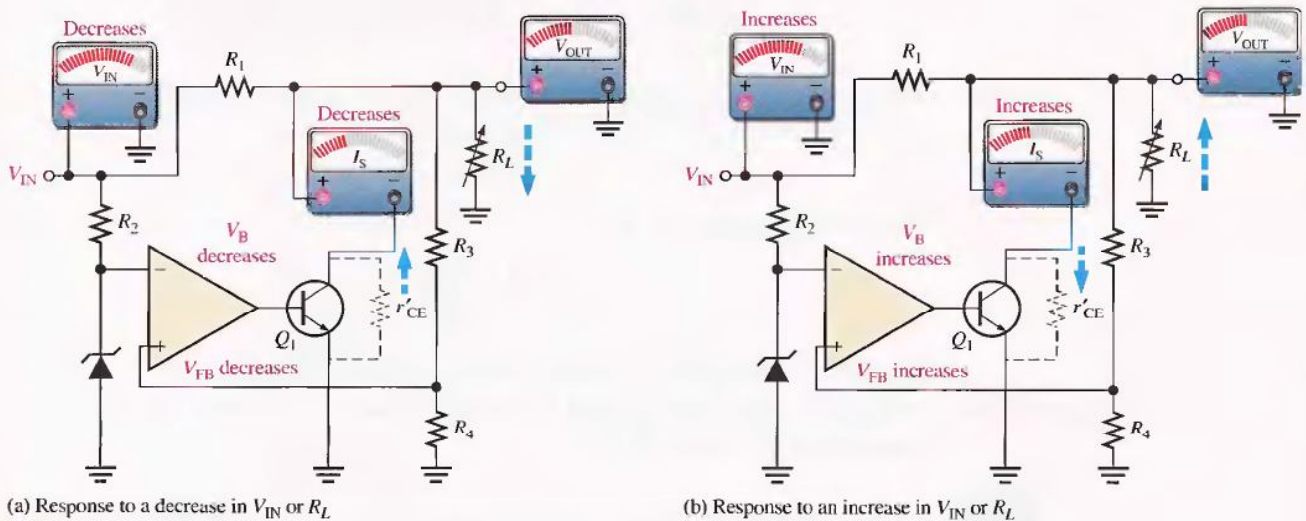
▲ FIGURE 18-12

Simple shunt regulator and block diagram.



▲ FIGURE 18-13

Basic op-amp shunt regulator with load resistor.



▲ FIGURE 18-14

Sequence of responses when V_{OUT} tries to decrease as a result of a decrease in R_L or V_{IN} (opposite responses for an attempted increase).

Since r_{CE}' acts as a voltage divider with R_1 , this action offsets the attempted decrease in V_{OUT} and maintains it at an almost constant level.

The opposite action occurs when the output tries to increase, as indicated in Figure 18–14(b). With I_L and V_{OUT} constant, a change in the input voltage produces a change in shunt current (I_S) as follows (Δ means “a change in”):

$$\Delta I_S = \frac{\Delta V_{IN}}{R_1}$$

With a constant V_{IN} and V_{OUT} , a change in load current causes an opposite change in shunt current. If I_L increases, I_S decreases, and vice versa.

$$\Delta I_S = -\Delta I_L$$

The shunt regulator is less efficient than the series type but offers inherent short-circuit protection. If the output is shorted ($V_{OUT} = 0$), the load current is limited by the series resistor R_1 to a maximum value as follows ($I_S = 0$).

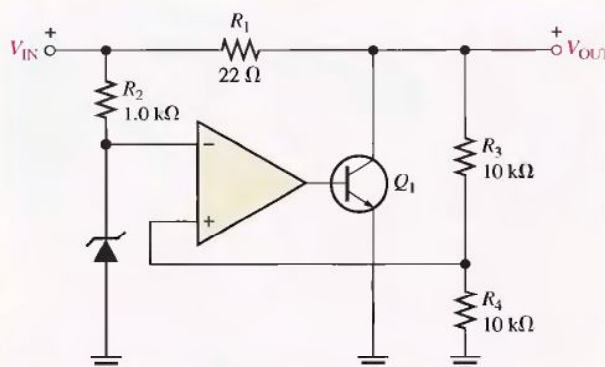
Equation 18–7

$$I_{L(max)} = \frac{V_{IN}}{R_1}$$

EXAMPLE 18–5

In Figure 18–15, what power rating must R_1 have if the maximum input voltage is 12.5 V?

► FIGURE 18–15



Solution The worst-case power dissipation in R_1 occurs when the output is short-circuited and $V_{OUT} = 0$. When $V_{IN} = 12.5$ V, the voltage dropped across R_1 is

$$V_{R1} = V_{IN} - V_{OUT} = 12.5 \text{ V}$$

The power dissipation in R_1 is

$$P_{R1} = \frac{V_{R1}^2}{R_1} = \frac{(12.5 \text{ V})^2}{22 \Omega} = 7.10 \text{ W}$$

Therefore, a resistor with a rating of at least 10 W should be used.

Related Problem In Figure 18–15, R_1 is changed to 33 Ω . What must be the power rating of R_1 if the maximum input voltage is 24 V?



Open the Multisim file E18-05 in the Examples folder on your CD-ROM. Measure the output voltage with 15 V applied to the input.

SECTION 18-3 REVIEW

1. How does the control element in a shunt regulator differ from that in a series regulator?
2. What is one advantage of a shunt regulator over a series type? What is a disadvantage?

18-4 BASIC SWITCHING REGULATORS

The two types of linear regulators, series and shunt, have control elements (transistors) that are conducting all the time, with the amount of conduction varied as demanded by changes in the output voltage or current. The switching regulator is different because the control element operates as a switch.

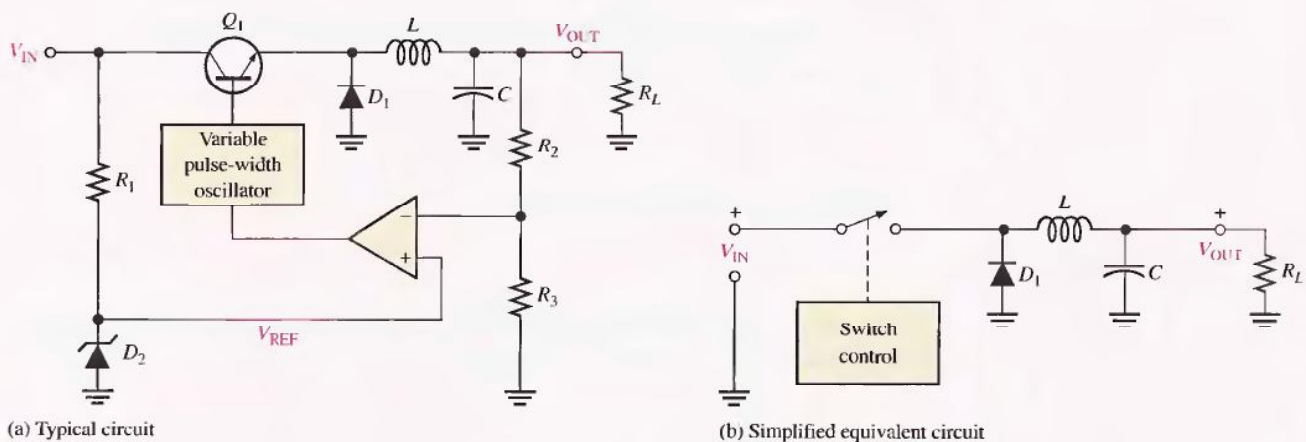
After completing this section, you should be able to

- Discuss the principles of switching regulators
- Describe the step-down configuration of a switching regulator
- Determine the output voltage of the step-down configuration
- Describe the step-up configuration of a switching regulator
- Describe the voltage-inverter configuration

A greater efficiency can be realized with a switching type of voltage regulator than with the linear types because the transistor is not always conducting. Therefore, switching regulators can provide greater load currents at low voltage than linear regulators because the control transistor doesn't dissipate as much power. Three basic configurations of switching regulators are step-down, step-up, and inverting.

Step-Down Configuration

In the step-down configuration, the output voltage is always less than the input voltage. A basic step-down **switching regulator** is shown in Figure 18-16(a), and its simplified equivalent is shown in Figure 18-16(b). Transistor Q_1 is used to switch the input voltage at a duty



▲ FIGURE 18-16

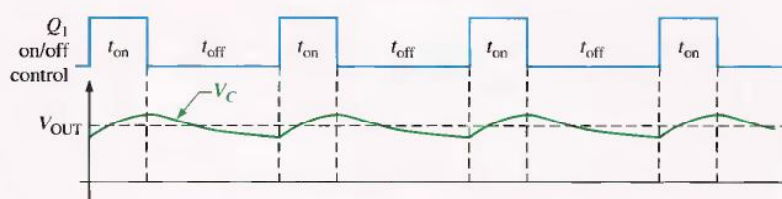
Basic step-down switching regulator.

cycle that is based on the regulator's load requirement. The LC filter is then used to average the switched voltage. Since Q_1 is either *on* (saturated) or *off*, the power lost in the control element is relatively small. Therefore, the switching regulator is useful primarily in higher power applications or in applications where efficiency is of utmost concern.

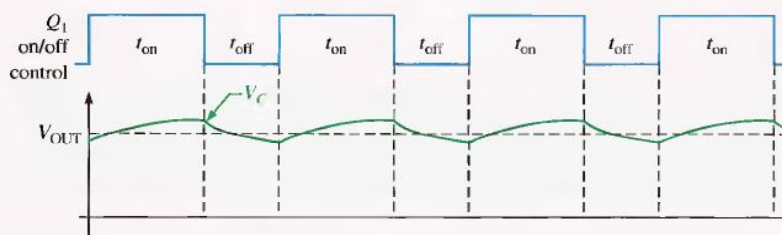
The *on* and *off* intervals of Q_1 are shown in the waveform of Figure 18-17(a). The capacitor charges during the on-time (t_{on}) and discharges during the off-time (t_{off}). When the on-time is increased relative to the off-time, the capacitor charges more, thus increasing the output voltage, as indicated in Figure 18-17(b). When the on-time is decreased relative to the off-time, the capacitor discharges more, thus decreasing the output voltage, as in Figure 18-17(c). The inductor further smooths the fluctuations of the output voltage caused by the charging and discharging action.

► **FIGURE 18-17**

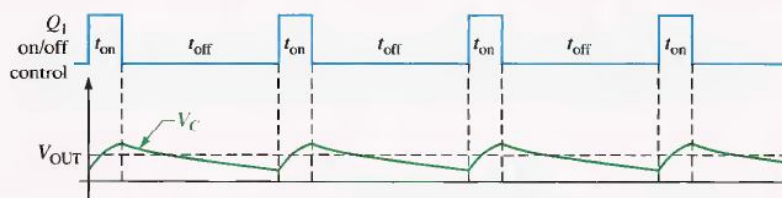
Switching regulator waveforms. The V_C waveform is shown for no inductive filtering to illustrate the charge and discharge action (ripple). L and C smooth V_C to a nearly constant level, as indicated by the dashed line for V_{OUT} .



(a) V_{OUT} depends on the duty cycle.



(b) Increase the duty cycle and V_{OUT} increases.



(c) Decrease the duty cycle and V_{OUT} decreases.

Ideally, the output voltage is expressed as

Equation 18-8

$$V_{OUT} = \left(\frac{t_{on}}{T} \right) V_{IN}$$

T is the period of the on-off cycle of Q_1 and is related to the frequency by $T = 1/f$. The period is the sum of the on-time and the off-time.

$$T = t_{on} + t_{off}$$

The ratio t_{on}/T is called the *duty cycle*.

The regulating action is as follows and is illustrated in Figure 18-18. When V_{OUT} tries to decrease, the on-time of Q_1 is increased, causing an additional charge on C to offset the at-

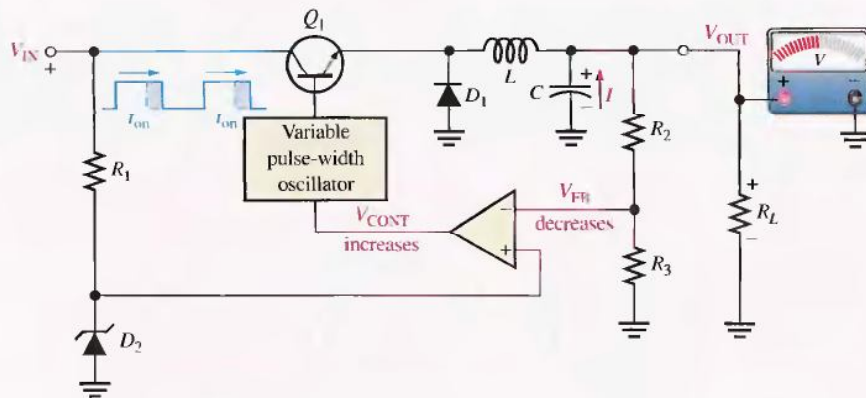
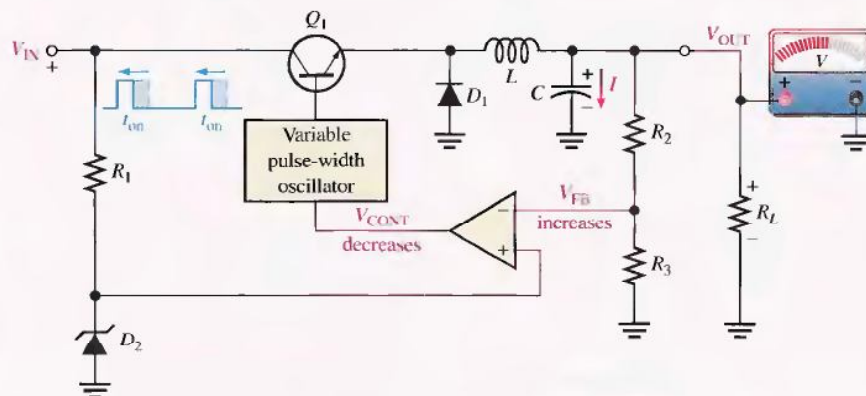


FIGURE 18-18

Basic regulating action of a step-down switching regulator.

(a) When V_{OUT} attempts to decrease, the on-time of Q_1 increases.



(b) When V_{OUT} attempts to increase, the on-time of Q_1 decreases.

tempted decrease. When V_{OUT} tries to increase, the on-time of Q_1 is decreased, causing the capacitor to discharge enough to offset the attempted increase.

Step-Up Configuration

A basic step-up type of switching regulator is shown in Figure 18-19, where transistor Q_1 operates as a switch to ground.

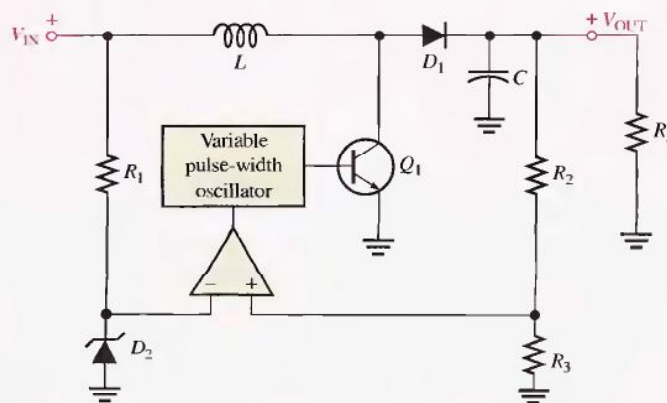


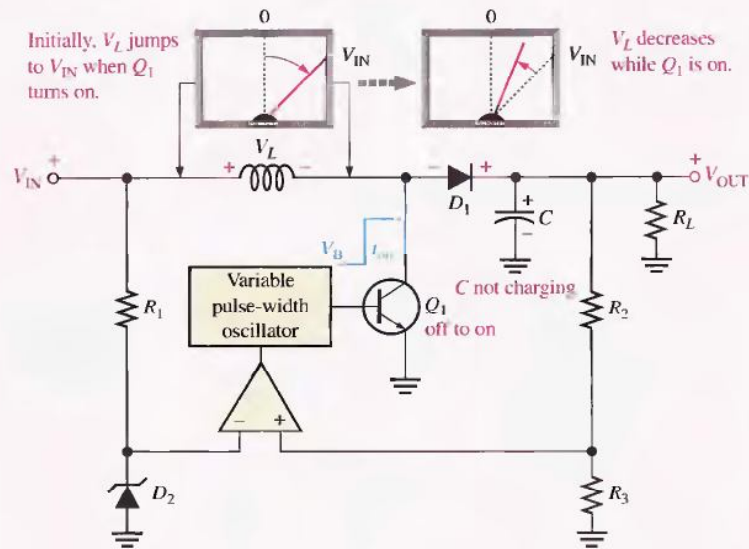
FIGURE 18-19

Basic step-up switching regulator.

The switching action is illustrated in Figures 18–20 and 18–21. When Q_1 turns on, a voltage equal to approximately V_{IN} is induced across the inductor with a polarity as indicated in Figure 18–20. During the on-time (t_{on}) of Q_1 , the inductor voltage, V_L , decreases from its initial maximum and diode D_1 is reverse-biased. The longer Q_1 is on, the smaller V_L becomes. During the on-time, the capacitor only discharges an extremely small amount through the load.

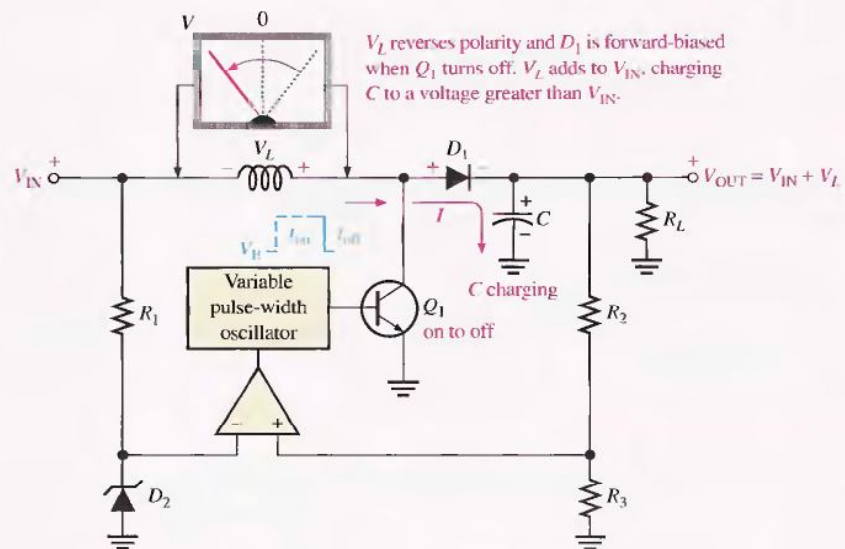
► **FIGURE 18–20**

Basic action of a step-up regulator when Q_1 is on.



► **FIGURE 18–21**

Basic switching action of a step-up regulator when Q_1 turns off.



When Q_1 turns off, as indicated in Figure 18–21, the inductor voltage suddenly reverses polarity and adds to V_{IN} , forward-biasing diode D_1 and allowing the capacitor to charge. The output voltage is equal to the capacitor voltage and can be larger than V_{IN} because the capacitor is charged to V_{IN} plus the voltage induced across the inductor during the off-time of Q_1 . The output voltage is dependent on both the inductor's magnetic field action (determined by t_{on}) and the charging of the capacitor (determined by t_{off}).

Voltage regulation is achieved by the variation of the on-time of Q_1 (within certain limits) as related to changes in V_{OUT} due to changing load or input voltage. If V_{OUT} tries to increase, the on-time of Q_1 will decrease, resulting in a decrease in the amount that C will

charge. If V_{OUT} tries to decrease, the on-time of Q_1 will increase, resulting in an increase in the amount that C will charge. This regulating action maintains V_{OUT} at an essentially constant level.

Voltage-Inverter Configuration

A third type of switching regulator produces an output voltage that is opposite in polarity to the input. A basic diagram is shown in Figure 18–22.

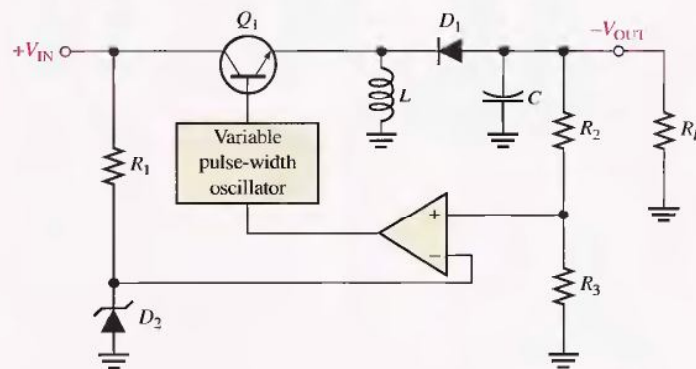
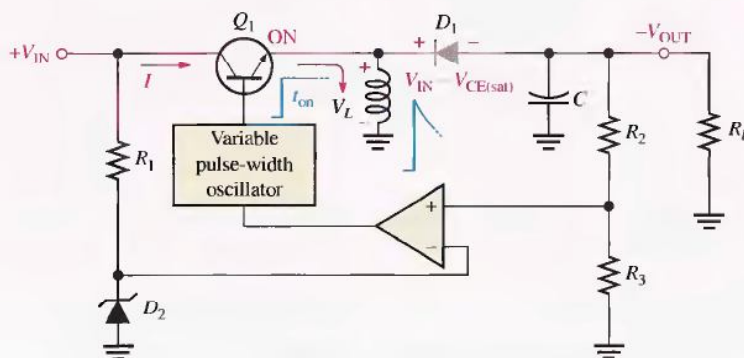
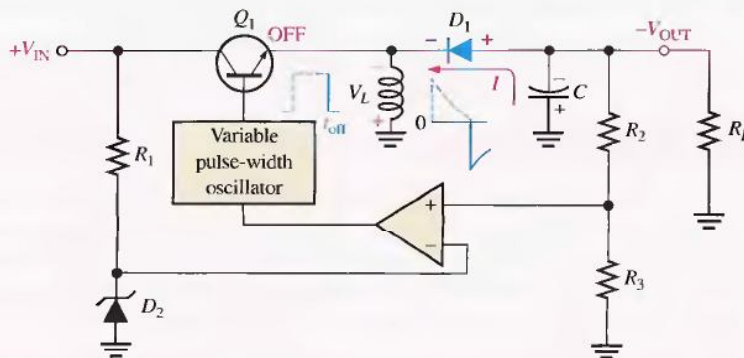


FIGURE 18–22
Basic inverting switching regulator.

When Q_1 turns on, the inductor voltage jumps to approximately $V_{IN} - V_{CE(sat)}$ and the magnetic field rapidly expands, as shown in Figure 18–23(a). While Q_1 is on, the diode is reverse-biased and the inductor voltage decreases from its initial maximum. When Q_1 turns off, the magnetic field collapses and the inductor's polarity reverses, as shown in Figure 18–23(b). This forward-biases the diode, charges C , and produces a negative output voltage, as indicated. The repetitive on-off action of Q_1 produces a repetitive charging and discharging that is smoothed by the LC filter action.



(a) When Q_1 is on, D_1 is reverse-biased.



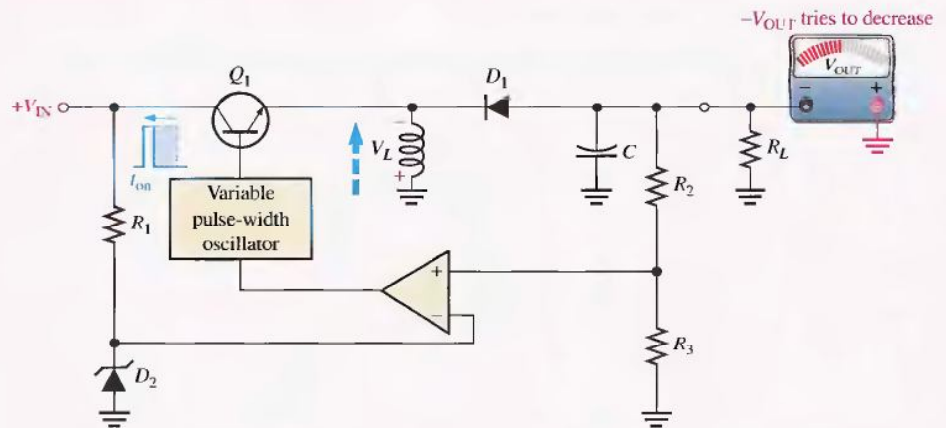
(b) When Q_1 turns off, D_1 forward biases.

FIGURE 18–23
Basic inverting action of an inverting switching regulator.

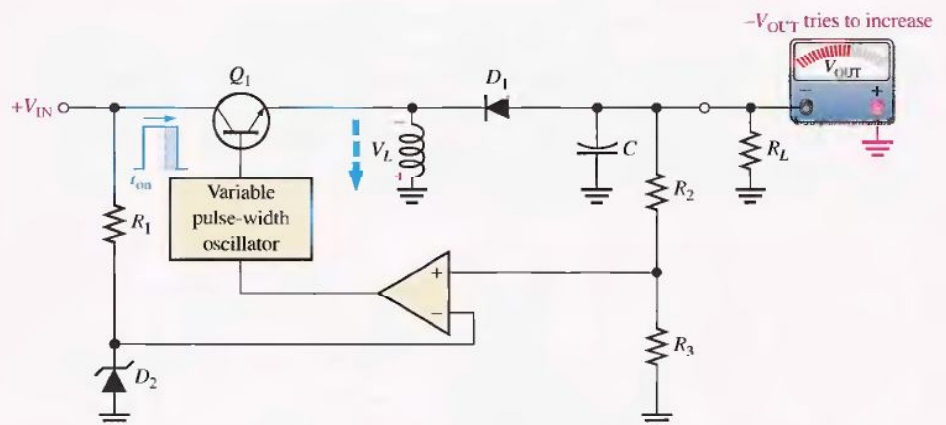
As with the step-up regulator, the less time Q_1 is on, the greater the output voltage is, and vice versa. This regulating action is illustrated in Figure 18–24. Switching regulator efficiencies can be greater than 90 percent.

► **FIGURE 18–24**

Basic regulating action of an inverting switching regulator.



(a) When $-V_{OUT}$ tries to decrease, t_{on} decreases, causing V_L to increase. This compensates for the attempted decrease in $-V_{OUT}$.



(b) When $-V_{OUT}$ tries to increase, t_{on} increases, causing V_L to decrease. This compensates for the attempted increase in $-V_{OUT}$.

SECTION 18–4 REVIEW

1. What are three types of switching regulators?
2. What is the primary advantage of switching regulators over linear regulators?
3. How are changes in output voltage compensated for in the switching regulator?

18–5 INTEGRATED CIRCUIT VOLTAGE REGULATORS

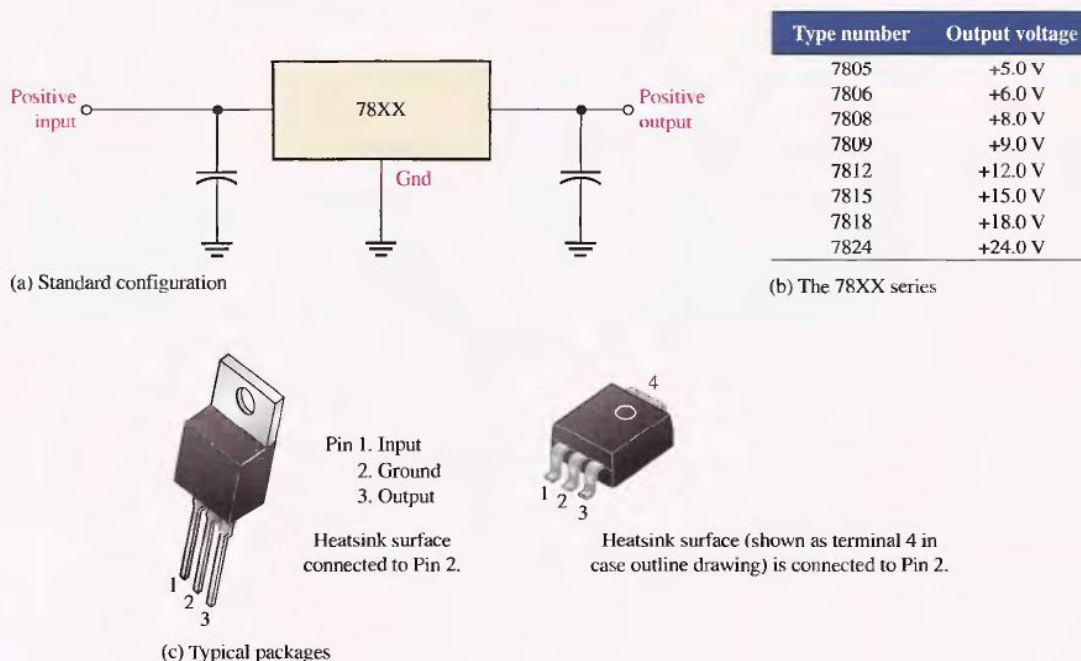
In the previous sections, the basic voltage regulator configurations were presented. Several types of both linear and switching regulators are available in integrated circuit (IC) form. Generally, the linear regulators are three-terminal devices that provide either positive or negative output voltages that can be either fixed or adjustable. In this section, typical linear and switching IC regulators are introduced.

After completing this section, you should be able to

- Discuss integrated circuit voltage regulators
- Describe the 78XX series of positive regulators
- Describe the 79XX series of negative regulators
- Describe the LM317 adjustable positive regulator
- Describe the LM337 adjustable negative regulator
- Describe IC switching regulators

Fixed Positive Linear Voltage Regulators

Although many types of IC regulators are available, the 78XX series of IC regulators is representative of three-terminal devices that provide a fixed positive output voltage. The three terminals are input, output, and ground as indicated in the standard fixed voltage configuration in Figure 18–25(a). The last two digits in the part number designate the output voltage. For example, the 7805 is a +5.0 V regulator. Other available output voltages are given in Figure 18–25(b) and common packages are shown in part (c).



▲ FIGURE 18–25

The 78XX series three-terminal fixed positive voltage regulators.

Capacitors, although not always necessary, are sometimes used on the input and output as indicated in Figure 18–25(a). The output capacitor acts basically as a line filter to improve transient response. The input capacitor is used to prevent unwanted oscillations when the regulator is some distance from the power supply filter such that the line has a significant inductance.

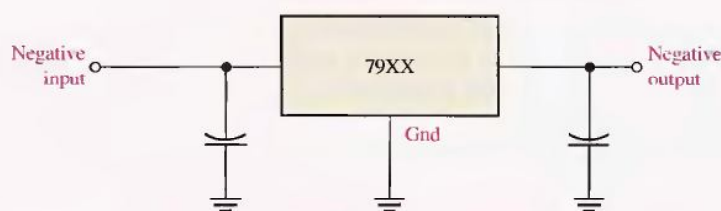
The 78XX series can produce output currents up to in excess of 1 A when used with an adequate heat sink. The input voltage must be at least 2 V above the output voltage in order



to maintain regulation. The circuits have internal thermal overload protection and short-circuit current-limiting features. **Thermal overload** occurs when the internal power dissipation becomes excessive and the temperature of the device exceeds a certain value. Almost all applications of regulators require that the device be secured to a heat sink to prevent thermal overload.

Fixed Negative Linear Voltage Regulators

The 79XX series is typical of three-terminal IC regulators that provide a fixed negative output voltage. This series is the negative-voltage counterpart of the 78XX series and shares most of the same features and characteristics. Figure 18–26 indicates the standard configuration and part numbers with corresponding output voltages that are available.



(a) Standard configuration

Type number	Output voltage
7905	–5.0 V
7905.2	–5.2 V
7906	–6.0 V
7908	–8.0 V
7912	–12.0 V
7915	–15.0 V
7918	–18.0 V
7924	–24.0 V

(b) The 79XX series

▲ FIGURE 18–26

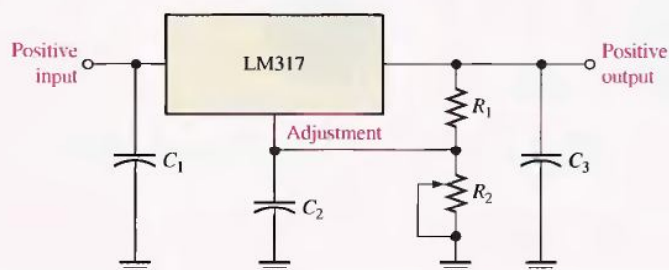
The 79XX series three-terminal fixed negative voltage regulators.

Adjustable Positive Linear Voltage Regulators

The LM317 is an example of a three-terminal positive regulator with an adjustable output voltage. The standard configuration is shown in Figure 18–27. The capacitors are for decoupling and do not affect the dc operation. Notice that there is an input, an output, and an adjustment terminal. The external fixed resistor R_1 and the external variable resistor R_2 provide the output voltage adjustment. V_{OUT} can be varied from 1.2 V to 37 V depending on the resistor values. The LM317 can provide over 1.5 A of output current to a load.

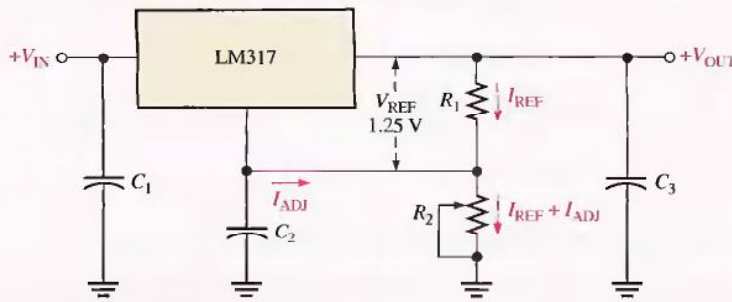
► FIGURE 18–27

The LM317 three-terminal adjustable positive voltage regulator.



The LM317 is operated as a “floating” regulator because the adjustment terminal is not connected to ground, but floats to whatever voltage is across R_2 . This allows the output voltage to be much higher than that of a fixed-voltage regulator.

Basic Operation As indicated in Figure 18–28, a constant 1.25 V reference voltage (V_{REF}) is maintained by the regulator between the output terminal and the adjustment terminal. This constant reference voltage produces a constant current (I_{REF}) through R_1 , regardless of the value of R_2 . I_{REF} is also through R_2 .


FIGURE 18-28

Operation of the LM317 adjustable voltage regulator.

$$I_{\text{REF}} = \frac{V_{\text{REF}}}{R_1} = \frac{1.25 \text{ V}}{R_1}$$

There is a very small constant current at the adjustment terminal of approximately $50 \mu\text{A}$ called I_{ADJ} , which is through R_2 . A formula for the output voltage is developed as follows.

$$\begin{aligned} V_{\text{OUT}} &= V_{R1} + V_{R2} = I_{\text{REF}}R_1 + I_{\text{REF}}R_2 + I_{\text{ADJ}}R_2 \\ &= I_{\text{REF}}(R_1 + R_2) + I_{\text{ADJ}}R_2 = \frac{V_{\text{REF}}}{R_1}(R_1 + R_2) + I_{\text{ADJ}}R_2 \end{aligned}$$

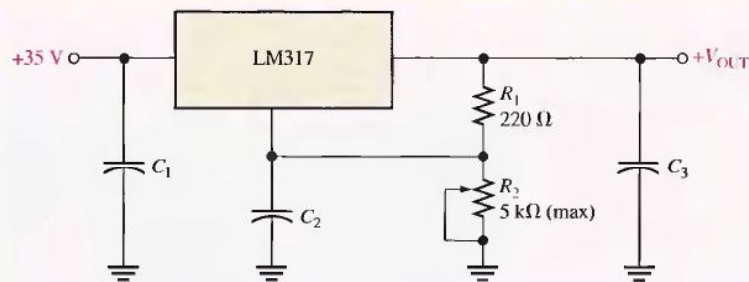
$$V_{\text{OUT}} = V_{\text{REF}} \left(1 + \frac{R_2}{R_1} \right) + I_{\text{ADJ}}R_2$$

Equation 18-9

As you can see, the output voltage is a function of both R_1 and R_2 . Once the value of R_1 is set, the output voltage is adjusted by varying R_2 .

EXAMPLE 18-6

Determine the minimum and maximum output voltages for the voltage regulator in Figure 18-29. Assume $I_{\text{ADJ}} = 50 \mu\text{A}$.

FIGURE 18-29

Solution

$$V_{R1} = V_{\text{REF}} = 1.25 \text{ V}$$

When R_2 is set at its minimum of 0Ω ,

$$V_{\text{OUT}(\text{min})} = V_{\text{REF}} \left(1 + \frac{R_2}{R_1} \right) + I_{\text{ADJ}}R_2 = 1.25 \text{ V}(1) = 1.25 \text{ V}$$

When R_2 is set at its maximum of 5 k Ω .

$$V_{OUT(max)} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2 = 1.25 \text{ V} \left(1 + \frac{5 \text{ k}\Omega}{220 \Omega} \right) + (50 \mu\text{A}) 5 \text{ k}\Omega$$

$$= 29.66 \text{ V} + 0.25 \text{ V} = \mathbf{29.9 \text{ V}}$$

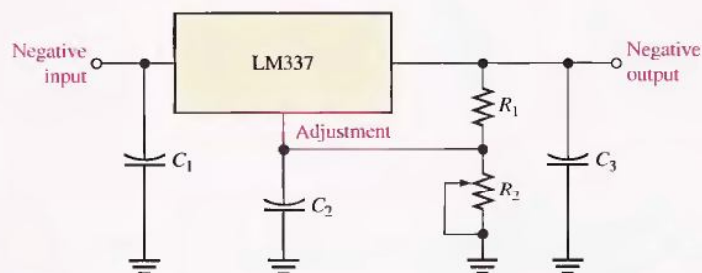
Related Problem What is the output voltage of the regulator if R_2 is set at 2 k Ω ?

Adjustable Negative Linear Voltage Regulators

The LM337 is the negative output counterpart of the LM317 and is a good example of this type of IC regulator. Like the LM317, the LM337 requires two external resistors for output voltage adjustment as shown in Figure 18–30. The output voltage can be adjusted from -1.2 V to -37 V , depending on the external resistor values. The capacitors are for decoupling and do not affect the dc operation.

FIGURE 18–30

The LM337 three-terminal adjustable negative voltage regulator.



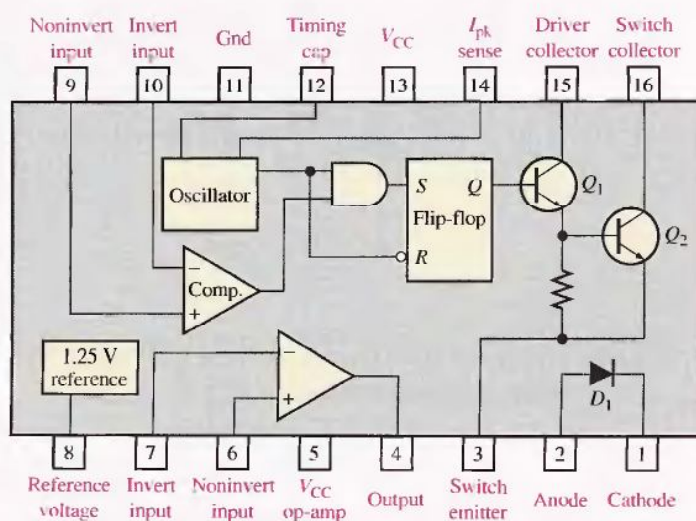
Switching Voltage Regulators

As an example of an IC switching voltage regulator, let's look at the 78S40. This is a universal device that can be used with external components to provide step-up, step-down, and inverting operation.

The internal circuitry of the 78S40 is shown in Figure 18–31. This circuit can be compared to the basic switching regulators that were covered in Section 18–4. For example,

FIGURE 18–31

The 78S40 switching regulator.



look back at Figure 18–16(a). The oscillator and comparator functions are directly comparable. The gate and flip-flop in the 78S40 were not included in the basic circuit of Figure 18–16(a), but they provide additional regulating action. Transistors Q_1 and Q_2 effectively perform the same function as Q_1 in the basic circuit. The 1.25 V reference block in the 78S40 has the same purpose as the zener diode in the basic circuit, and diode D_1 in the 78S40 corresponds to D_1 in the basic circuit.

The 78S40 also has an “uncommitted” op-amp thrown in for good measure. It is not used in any of the regulator configurations. External circuitry is required to make this device operate as a regulator, as you will see in Section 18–6.

SECTION 18–5 REVIEW

1. What are the three terminals of a fixed-voltage regulator?
2. What is the output voltage of a 7809? Of a 7915?
3. What are the three terminals of an adjustable-voltage regulator?
4. What external components are required for a basic LM317 configuration?

18–6 APPLICATIONS OF IC VOLTAGE REGULATORS

In the last section, you saw several devices that are representative of the general types of IC voltage regulators. Now, several different ways these devices can be modified with external circuitry to improve or alter their performance are examined.

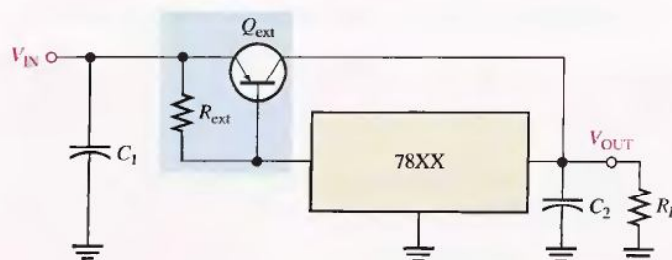
After completing this section, you should be able to

- Discuss applications of IC voltage regulators
- Explain the use of an external pass transistor
- Explain the use of current limiting
- Explain how to use a voltage regulator as a constant-current source
- Discuss some application considerations for switching regulators

The External Pass Transistor

As you know, an IC voltage regulator is capable of delivering only a certain amount of output current to a load. For example, the 78XX series regulators can handle a peak output current of 1.3 A (more under certain conditions). If the load current exceeds the maximum allowable value, there will be thermal overload and the regulator will shut down. A thermal overload condition means that there is excessive power dissipation inside the device.

If an application requires more than the maximum current that the regulator can deliver, an external pass transistor Q_{ext} can be used. Figure 18–32 illustrates a three-terminal regulator



◀ **FIGURE 18–32**

A 78XX-series three-terminal regulator with an external pass transistor to increase power dissipation.

with an external pass transistor for handling currents in excess of the output current capability of the basic regulator.

The value of the external current-sensing resistor, R_{ext} , determines the value of current at which Q_{ext} begins to conduct because it sets the base-to-emitter voltage of the transistor. As long as the current is less than the value set by R_{ext} , the transistor Q_{ext} is off, and the regulator operates normally as shown in Figure 18–33(a). This is because the voltage drop across R_{ext} is less than the 0.7 V base-to-emitter voltage required to turn Q_{ext} on. R_{ext} is determined by the following formula, where I_{max} is the highest current that the voltage regulator is to handle internally.

Equation 18–10

$$R_{\text{ext}} = \frac{0.7 \text{ V}}{I_{\text{max}}}$$

When the current is sufficient to produce at least a 0.7 V drop across R_{ext} , the external pass transistor Q_{ext} turns on and conducts any current in excess of I_{max} , as indicated in Figure 18–33(b). Q_{ext} will conduct more or less, depending on the load requirements. For example, if the total load current is 3 A and I_{max} was selected to be 1 A, the external pass transistor will conduct 2 A, which is the excess over the internal voltage regulator current I_{max} .

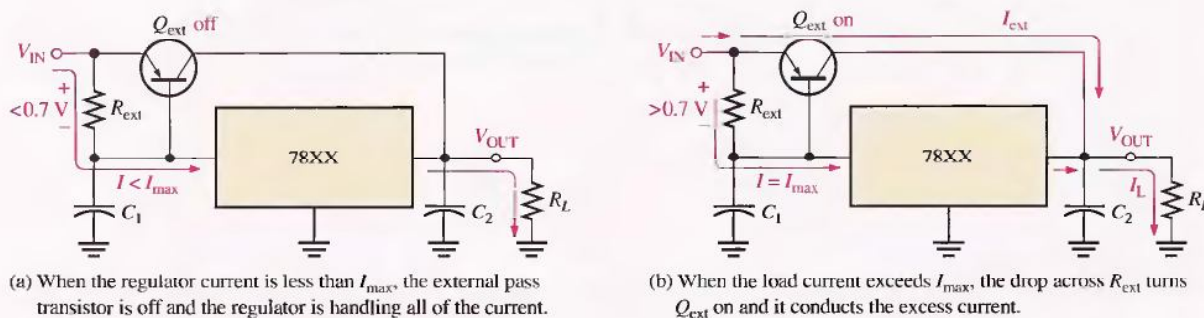


FIGURE 18–33

Operation of the regulator with an external pass transistor.

EXAMPLE 18–7

What value is R_{ext} if the maximum current to be handled internally by the voltage regulator in Figure 18–32 is set at 700 mA?

Solution

$$R_{\text{ext}} = \frac{0.7 \text{ V}}{I_{\text{max}}} = \frac{0.7 \text{ V}}{0.7 \text{ A}} = 1 \Omega$$

Related Problem

If R_{ext} is changed to 1.5 Ω , at what current value will Q_{ext} turn on?

The external pass transistor is typically a power transistor with a heat sink that must be capable of handling a maximum power of

$$P_{\text{ext}} = I_{\text{ext}}(V_{\text{IN}} - V_{\text{OUT}})$$

EXAMPLE 18-8

What must be the minimum power rating for the external pass transistor used with a 7824 regulator in a circuit such as that shown in Figure 18-32? The input voltage is 30 V and the load resistance is 10 Ω . The maximum internal current is to be 700 mA. Assume that there is no heat sink for this calculation. Keep in mind that the use of a heat sink increases the effective power rating of the transistor and you can use a lower rated transistor.

Solution The load current is

$$I_L = \frac{V_{OUT}}{R_L} = \frac{24 \text{ V}}{10 \Omega} = 2.4 \text{ A}$$

The current through Q_{ext} is

$$I_{ext} = I_L - I_{max} = 2.4 \text{ A} - 0.7 \text{ A} = 1.7 \text{ A}$$

The power dissipated by Q_{ext} is

$$P_{ext(min)} = I_{ext}(V_{IN} - V_{OUT}) = (1.7 \text{ A})(30 \text{ V} - 24 \text{ V}) = (1.7 \text{ A})(6 \text{ V}) = 10.2 \text{ W}$$

For a safety margin, choose a power transistor with a rating greater than 10.2 W, say at least 15 W.

Related Problem Rework this example using a 7815 regulator.

Current Limiting

A drawback of the circuit in Figure 18-32 is that the external transistor is not protected from excessive current, such as would result from a shorted output. An additional current-limiting circuit (Q_{lim} and R_{lim}) can be added as shown in Figure 18-34 to protect Q_{ext} from excessive current and possible burn out.

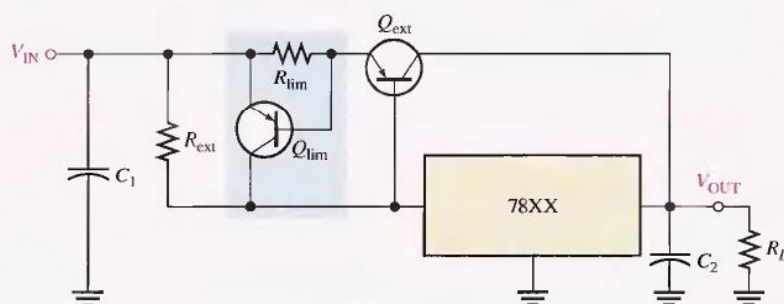


FIGURE 18-34

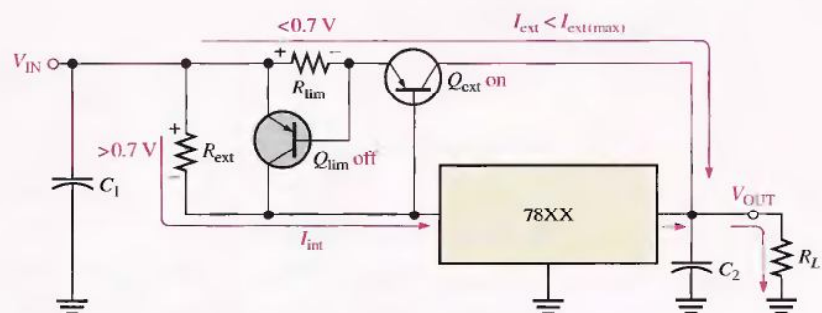
Regulator with current limiting.

The following describes the way the current-limiting circuit works. The current-sensing resistor R_{lim} sets the V_{BE} of transistor Q_{lim} . The base-to-emitter voltage of Q_{ext} is now determined by $V_{R_{ext}} - V_{R_{lim}}$ because they have opposite polarities. So, for normal operation, the drop across R_{ext} must be sufficient to overcome the opposing drop across R_{lim} . If the current through Q_{ext} exceeds a certain maximum ($I_{ext(max)}$) because of a shorted output or a faulty load, the voltage across R_{lim} reaches 0.7 V and turns Q_{lim} on. Q_{lim} now conducts current through the regulator and away from Q_{ext} , forcing a thermal overload to occur and shut down the regulator. Remember, the IC regulator is internally protected from thermal overload as part of its design.

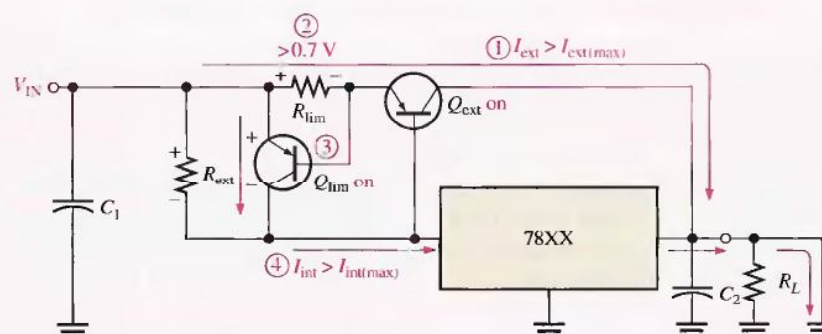
This action is illustrated in Figure 18–35. In part (a), the circuit is operating normally with Q_{ext} conducting less than the maximum current that it can handle with Q_{lim} off. Part (b) shows what happens when there is a short across the load. The current through Q_{ext} suddenly increases and causes the voltage drop across R_{lim} to increase, which turns Q_{lim} on. The current is now diverted through the regulator, which causes it to shut down due to thermal overload.

► **FIGURE 18–35**

The current-limiting action of the regulator circuit.



(a) During normal operation, when the load current is not excessive, Q_{lim} is off.



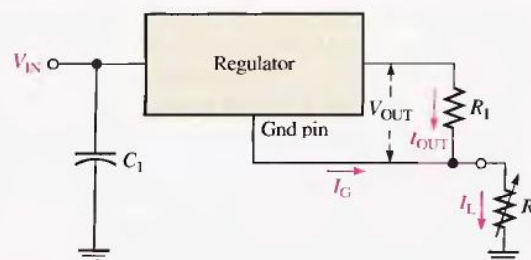
(b) When short occurs (1), the external current becomes excessive and the voltage across R_{lim} increases (2) and turns on Q_{lim} (3), which then routes current through the regulator and conducts it away from Q_{ext} , causing the internal regulator current to become excessive (4) which forces the regulator into thermal shut down.

A Current Regulator

The three-terminal regulator can be used as a current source when an application requires that a constant current be supplied to a variable load. The basic circuit is shown in Figure 18–36 where R_1 is the current-setting resistor. The regulator provides a fixed constant volt-

► **FIGURE 18–36**

The three-terminal regulator as a current source.



age, V_{OUT} , between the ground terminal (not connected to ground in this case) and the output terminal. This determines the constant current supplied to the load.

$$I_L = \frac{V_{OUT}}{R_1} + I_G$$

Equation 18-11

The current, I_G , from the ground terminal is very small compared to the output current and can often be neglected.

EXAMPLE 18-9

What value of R_1 is necessary in a 7805 regulator to provide a constant current of 1 A to a variable load that can be adjusted from 1 Ω to 10 Ω ?

Solution First, 1 A is within the limits of the 7805's capability (remember, it can handle at least 1.3 A without an external pass transistor).

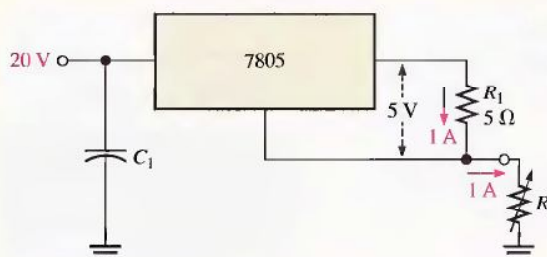
The 7805 produces 5 V between its ground terminal and its output terminal. Therefore, if you want 1 A of current, the current-setting resistor must be (neglecting I_G)

$$R_1 = \frac{V_{OUT}}{I_L} = \frac{5 \text{ V}}{1 \text{ A}} = 5 \Omega$$

The circuit is shown in Figure 18-37.

FIGURE 18-37

A constant-current source of 1 A.



Related Problem If a 7808 regulator is used instead of the 7805, to what value would you change R_1 to maintain a constant current of 1 A?

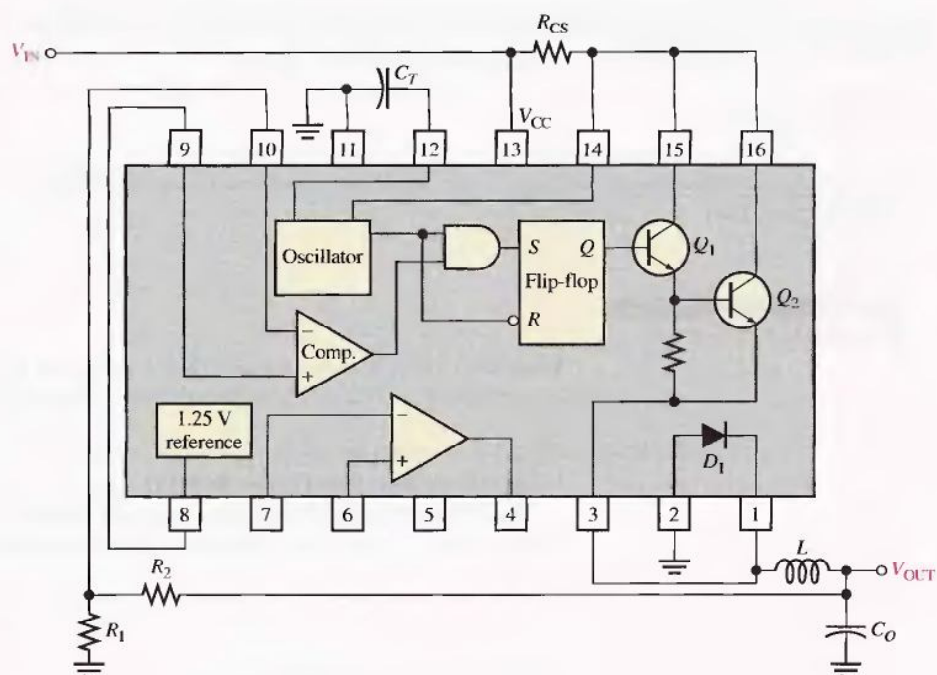
Switching Regulator Configurations

In Section 18-5, the 78S40 was introduced as an example of an IC switching voltage regulator. Figure 18-38 shows the external connections for a step-down configuration where the output voltage is less than the input voltage, and Figure 18-39 shows a step-up configuration in which the output voltage is greater than the input voltage. An inverting configuration is also possible, but it is not shown here.

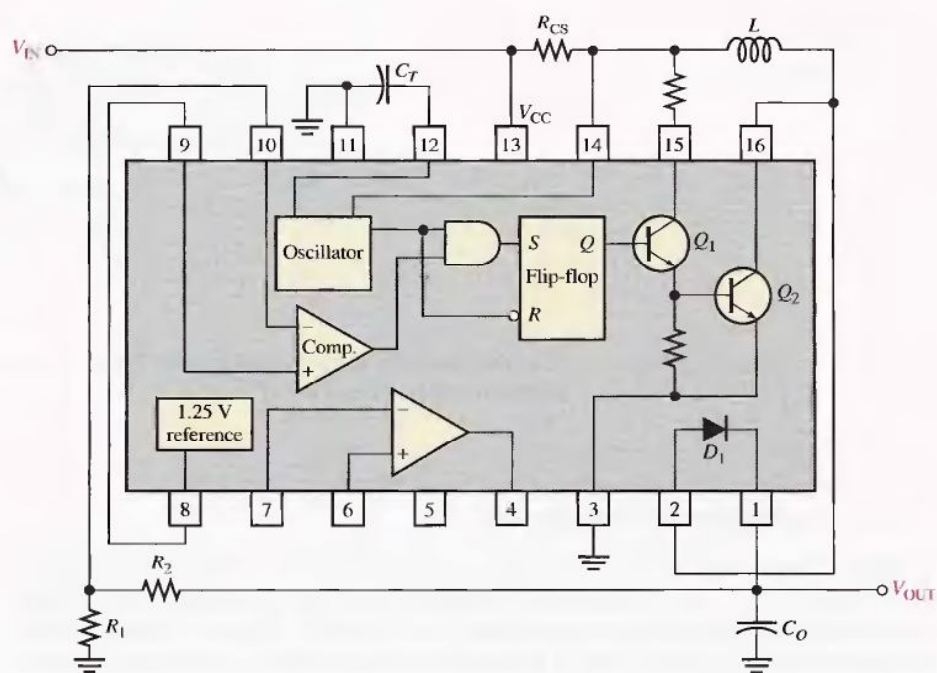
The timing capacitor, C_T , controls the pulse width and frequency of the oscillator and thus establishes the on-time of transistor Q_2 . The voltage across the current-sensing resistor, R_{CS} , is used internally by the oscillator to vary the duty cycle based on the desired peak load current. The voltage divider, made up of R_1 and R_2 , reduces the output voltage to a nominal value equal to the reference voltage. If V_{OUT} exceeds its set value, the output of the comparator switches to its low state, disabling the gate to turn Q_2 off until the output decreases. This regulating action is in addition to that produced by the duty cycle variation of the oscillator as described in Section 18-4 in relation to the basic switching regulator.

► **FIGURE 18-38**

The step-down configuration of the 78S40 switching regulator.

► **FIGURE 18-39**

The step-up configuration of the 78S40 switching regulator.



SECTION 18-6 REVIEW

1. What is the purpose of using an external pass transistor with an IC voltage regulator?
2. What is the advantage of current limiting in a voltage regulator?
3. What does *thermal overload* mean?



SYSTEM APPLICATION

The regulated power supply in this application provides dual-polarity dc voltages of ± 12 V to the FM receiver system which you worked with in Chapter 15. The power supply consists of a transformer-coupled full-wave bridge rectifier and filter with positive and negative three-terminal voltage regulators.

The block diagram of the dual-polarity power supply is shown in Figure 18-40, and the circuit board is shown in Figure 18-41. The large vertically mounted capacitors are the 100 μ F filter capacitors. The 0.33 μ F and 1 μ F capacitors, although not necessary in all applications, are recommended by the manufacturer for stability and improved transient response.

The Dual-Polarity Power Supply Board

- Make sure that the circuit board shown in Figure 18-41 is correct by checking it against the schematic in Figure 18-42. Backside interconnections are shown as darker traces.
- Label a copy of the board with component and input/output designations in agreement with the schematic.

The Power Supply Circuit

- Determine the approximate voltage at each of the four "corners" of the bridge. The transformer is rated at 24 V rms.
- Calculate the peak inverse voltage of the rectifier diodes.
- Determine the voltage at the input of each voltage regulator.
- In the FM receiver from Chapter 15, assume that op-amps are used only in the channel separation circuits. If all the other circuits in the receiver, excluding the channel separation circuits, used +12 V only and draw an average dc current of 100 mA, determine how much total current each regulator must supply.

- Based on the amount of dc current required by the receiver, do the regulators need to be attached to the heat sink?

Test Procedure

Develop a basic procedure for thoroughly testing the dual-polarity power supply.

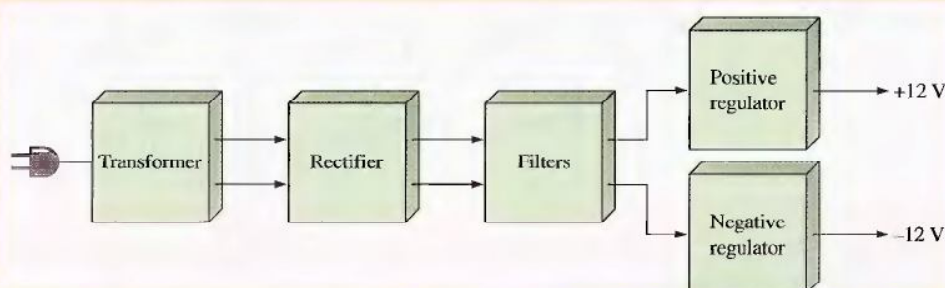
Troubleshooting

Based on the results indicated in Figure 18-43 for four faulty power supply boards, determine the most likely fault or faults in each case.

Final Report (Optional)

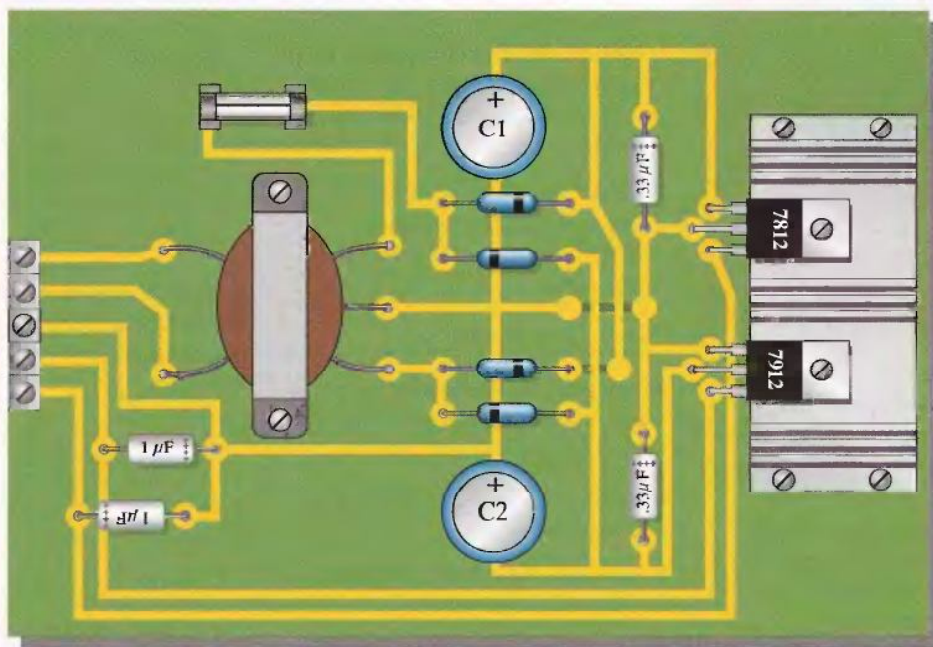
Submit a final written report on the dual-polarity power supply using an organized format that includes the following:

1. A physical description of the circuit.
2. A discussion of the operation of the circuit.
3. A list of the specifications.
4. A list of parts with part numbers if available.
5. A list of the types of problems in the four faulty boards.



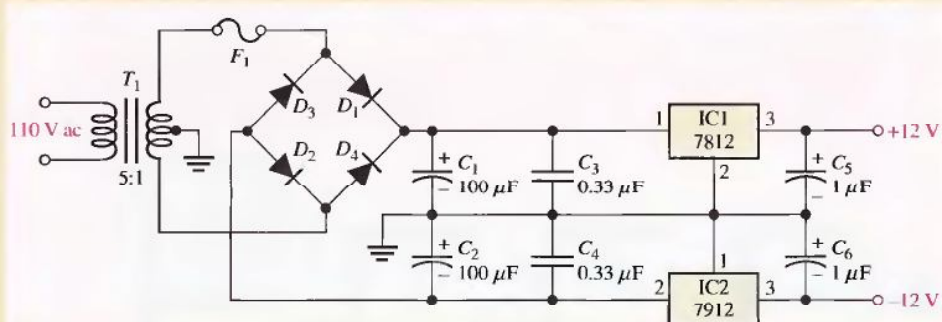
▲ FIGURE 18-40

Block diagram of the dual-polarity power supply.



▲ **FIGURE 18-41**

The dual-polarity power supply circuit board.



▲ **FIGURE 18-42**

The dual-polarity power supply schematic.

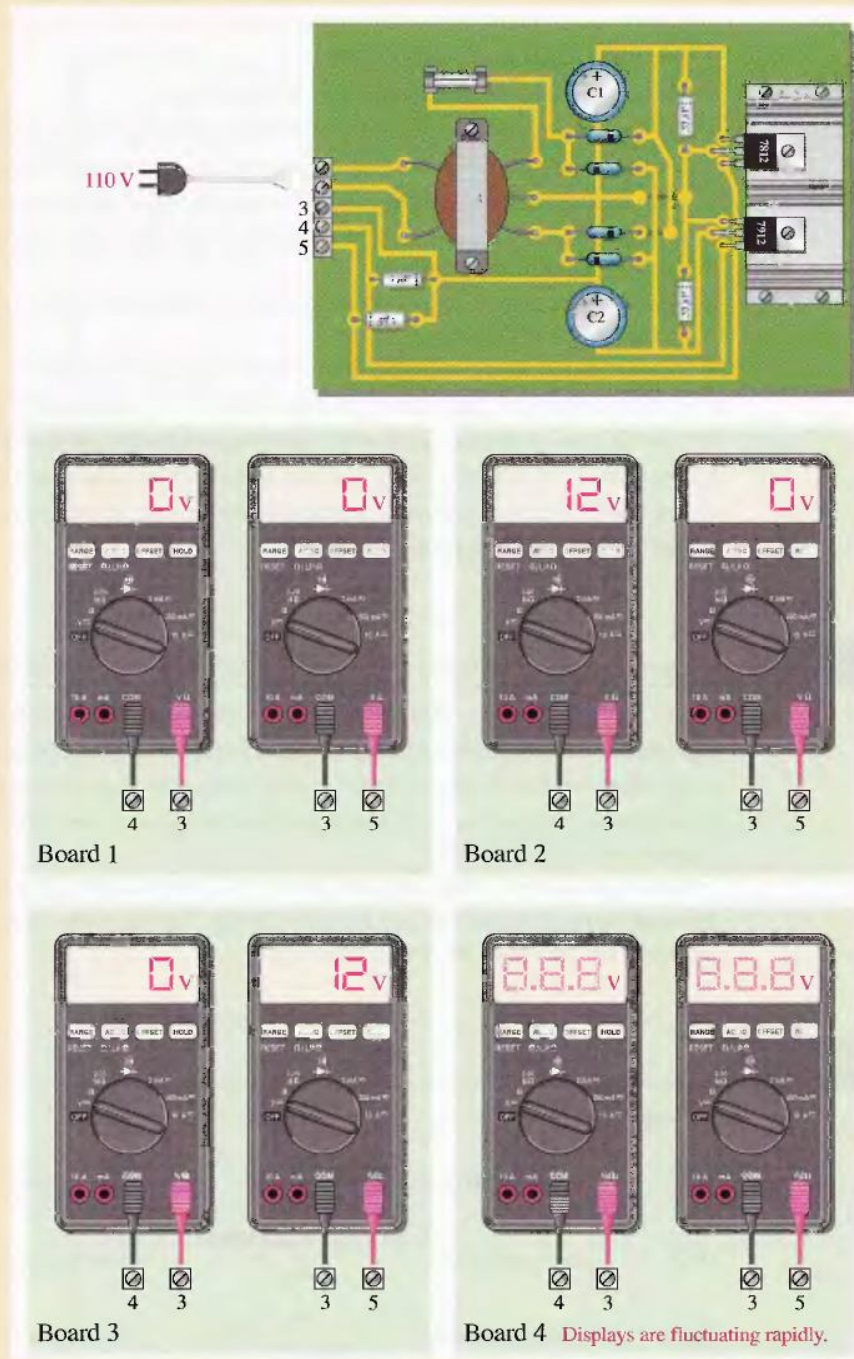


FIGURE 18-43

Results of tests on four faulty power supply boards.

CHAPTER SUMMARY

- Voltage regulators keep a constant dc output voltage when the input or load varies within limits.
- A basic voltage regulator consists of a reference voltage source, an error detector, a sampling element, and a control device. Protection circuitry is also found in most regulators.
- Two basic categories of voltage regulators are linear and switching.
- Two basic types of linear regulators are series and shunt.
- In a series linear regulator, the control element is a transistor in series with the load.
- In a shunt linear regulator, the control element is a transistor in parallel with the load.
- Three configurations for switching regulators are step-down, step-up, and inverting.
- Switching regulators are more efficient than linear regulators and are particularly useful in low-voltage, high-current applications.
- Three-terminal linear IC regulators are available for either fixed output or variable output voltages of positive or negative polarities.
- An external pass transistor increases the current capability of a regulator.
- The 78XX series are three-terminal IC regulators with fixed positive output voltage.
- The 79XX series are three-terminal IC regulators with fixed negative output voltage.
- The LM317 is a three-terminal IC regulator with a positive variable output voltage.
- The LM337 is a three-terminal IC regulator with a negative variable output voltage.
- The 78S40 is a switching voltage regulator.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Linear regulator A voltage regulator in which the control element operates in the linear region.

Line regulation The percentage change in output voltage for a given change in input (line) voltage.

Load regulation The percentage change in output voltage for a given change in load current.

Regulator An electronic circuit that maintains an essentially constant output voltage with a changing input voltage or load current.

Switching regulator A voltage regulator in which the control element operates as a switch.

Thermal overload A condition in a rectifier where the internal power dissipation of the circuit exceeds a certain maximum due to excessive current.

KEY FORMULAS

Voltage Regulation

18-1	$\text{Line regulation} = \left(\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right) 100\%$	Line regulation as a percentage
18-2	$\text{Line regulation} = \frac{(\Delta V_{\text{OUT}}/V_{\text{OUT}}) 100\%}{\Delta V_{\text{IN}}}$	Line regulation in %/V
18-3	$\text{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \right) 100\%$	Percent load regulation
18-4	$\text{Load regulation} = \left(\frac{R_{\text{OUT}}}{R_{\text{FL}}} \right) 100\%$	Load regulation in terms of output resistance and full-load resistance

Basic Series Regulator

18-5	$V_{\text{OUT}} \cong \left(1 + \frac{R_2}{R_3} \right) V_{\text{REF}}$	Regulator output
------	--	------------------

$$18-6 \quad I_{L(\max)} = \frac{0.7 \text{ V}}{R_4}$$

For constant-current limiting
(silicon)

Basic Shunt Regulator

$$18-7 \quad I_{L(\max)} = \frac{V_{IN}}{R_1}$$

Maximum load current

Basic Switching Regulators

$$18-8 \quad V_{OUT} = \left(\frac{t_{on}}{T} \right) V_{IN}$$

For step-down switching regulator

IC Voltage Regulators

$$18-9 \quad V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

IC regulator

$$18-10 \quad R_{ext} = \frac{0.7 \text{ V}}{I_{max}}$$

For external pass circuit

$$18-11 \quad I_L = \frac{V_{OUT}}{R_1} + I_G$$

Regulator as a current source

CIRCUIT-ACTION QUIZ

Answers are at the end of the chapter.

- If the input voltage in Figure 18-7 is increased by 1 V, the output voltage will
(a) increase (b) decrease (c) not change
- If the zener diode in Figure 18-7 is changed to one with a zener voltage of 6.8 V, the output voltage will
(a) increase (b) decrease (c) not change
- If R_3 in Figure 18-7 is increased in value, the output voltage will
(a) increase (b) decrease (c) not change
- If R_4 in Figure 18-9 is reduced, the amount of current that the regulator can supply to the load will
(a) increase (b) decrease (c) not change
- If R_2 in Figure 18-15 is increased, the power dissipation in R_1 will
(a) increase (b) decrease (c) not change
- If the duty cycle of the variable pulse-width oscillator in Figure 18-16(a) is increased, the output voltage will
(a) increase (b) decrease (c) not change
- If R_2 in Figure 18-29 is adjusted to a lower value, the output voltage will
(a) increase (b) decrease (c) not change
- To increase the maximum current that the regulator in Figure 18-33 can supply, the value of R_{ext} must
(a) increase (b) decrease (c) not change

SELF-TEST

Answers are at the end of the chapter.

- In the case of line regulation,
(a) when the temperature varies, the output voltage stays constant
(b) when the output voltage changes, the load current stays constant
(c) when the input voltage changes, the output voltage stays constant
(d) when the load changes, the output voltage stays constant

2. In the case of load regulation,
 - (a) when the temperature varies, the output voltage stays constant
 - (b) when the input voltage changes, the load current stays constant
 - (c) when the load changes, the load current stays constant
 - (d) when the load changes, the output voltage stays constant
3. All of the following are parts of a basic voltage regulator *except*
 - (a) control element (b) sampling circuit
 - (c) voltage-follower (d) error detector (e) reference voltage
4. The basic difference between a series regulator and a shunt regulator is
 - (a) the amount of current that can be handled (b) the position of the control element
 - (c) the type of sample circuit (d) the type of error detector
5. In a basic series regulator, V_{OUT} is determined by
 - (a) the control element (b) the sample circuit
 - (c) the reference voltage (d) answers (b) and (c)
6. The main purpose of current limiting in a regulator is
 - (a) protection of the regulator from excessive current
 - (b) protection of the load from excessive current
 - (c) to keep the power supply transformer from burning up
 - (d) to maintain a constant output voltage
7. In a linear regulator, the control transistor is conducting
 - (a) a small part of the time (b) half the time
 - (c) all of the time (d) only when the load current is excessive
8. In a switching regulator, the control transistor is conducting
 - (a) part of the time (b) all of the time
 - (c) only when the input voltage exceeds a set limit (d) only when there is an overload
9. The LM317 is an example of an IC
 - (a) three-terminal negative voltage regulator (b) fixed positive voltage regulator
 - (c) switching regulator (d) linear regulator
 - (e) variable positive voltage regulator (f) answers (b) and (d) only
 - (g) answers (d) and (e) only
10. An external pass transistor is used for
 - (a) increasing the output voltage (b) improving the regulation
 - (c) increasing the current that the regulator can handle (d) short-circuit protection

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

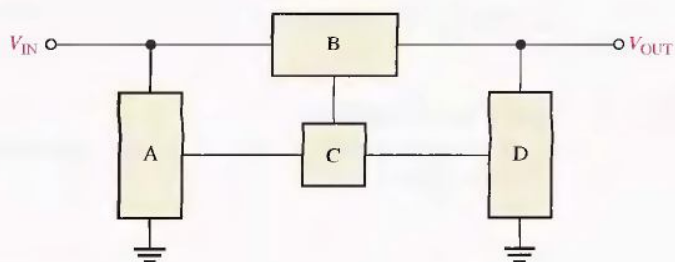
SECTION 18-1 Voltage Regulation

1. The nominal output voltage of a certain regulator is 8 V. The output changes 2 mV when the input voltage goes from 12 V to 18 V. Determine the line regulation and express it as a percentage change over the entire range of V_{IN} .
2. Express the line regulation found in Problem 1 in units of %/V.
3. A certain regulator has a no-load output voltage of 10 V and a full-load output voltage of 9.90 V. What is the percent load regulation?
4. In Problem 3, if the full-load current is 250 mA, express the load regulation in %/mA.

SECTION 18-2 Basic Series Regulators

5. Label the functional blocks for the voltage regulator in Figure 18-44.

FIGURE 18-44

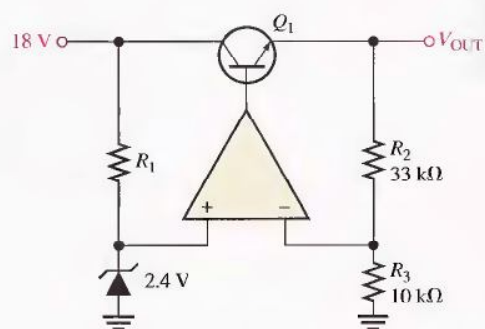


6. Determine the output voltage for the regulator in Figure 18-45.



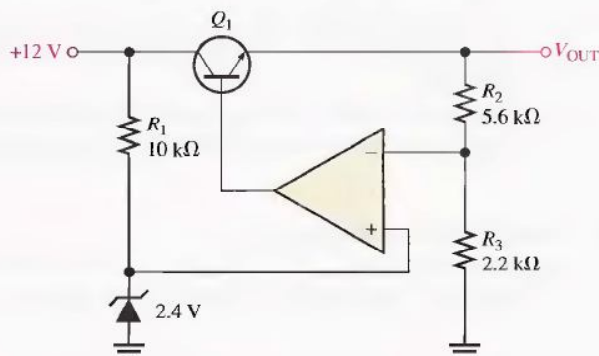
FIGURE 18-45

Multisim file circuits are identified with a CD logo and are in the Problems folder on your CD-ROM. Filenames correspond to figure numbers (e.g., F18-45).



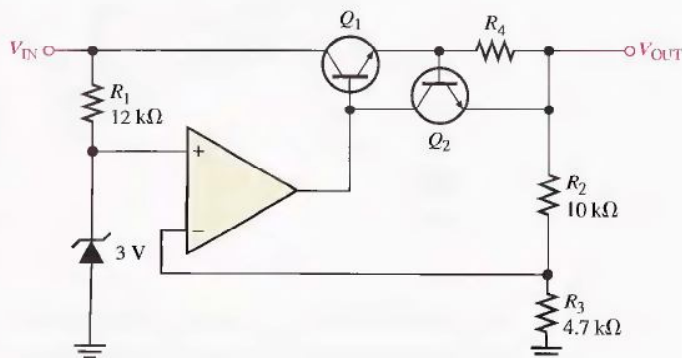
7. Determine the output voltage for the series regulator in Figure 18-46.

FIGURE 18-46



8. If R_3 in Figure 18-46 is increased to 4.7 kΩ, what happens to the output voltage?
9. If the zener voltage is 2.7 V instead of 2.4 V in Figure 18-46, what is the output voltage?
10. A series voltage regulator with constant-current limiting is shown in Figure 18-47. Determine the value of R_4 if the load current is to be limited to a maximum value of 250 mA. What power rating must R_4 have?

FIGURE 18-47

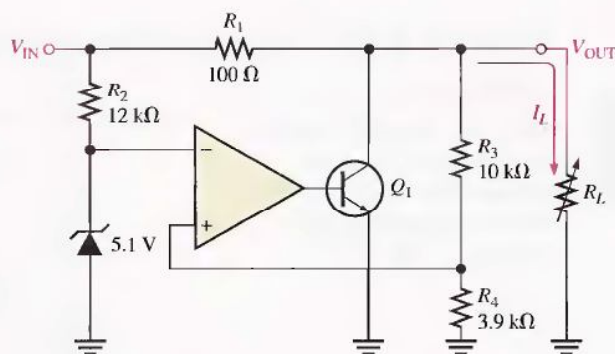


11. If the R_4 determined in Problem 10 is halved, what is the maximum load current?

SECTION 18-3 Basic Shunt Regulators

12. In the shunt regulator of Figure 18-48, when the load current increases, does Q_1 conduct more or less? Why?

► FIGURE 18-48

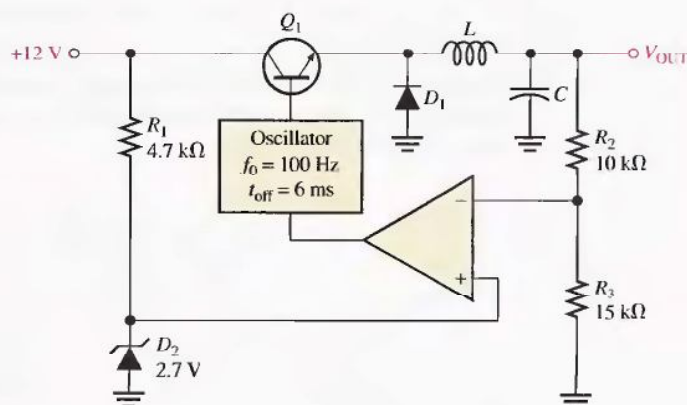


13. Assume I_L remains constant and V_{IN} changes by 1 V in Figure 18-48. What is the change in the collector current of Q_1 ?
14. With a constant input voltage of 17 V, the load resistance in Figure 18-48 is varied from 1 kΩ to 1.2 kΩ. Neglecting any change in output voltage, how much does the shunt current through Q_1 change?
15. If the maximum allowable input voltage in Figure 18-48 is 25 V, what is the maximum possible output current when the output is short-circuited? What power rating should R_1 have?

SECTION 18-4 Basic Switching Regulators

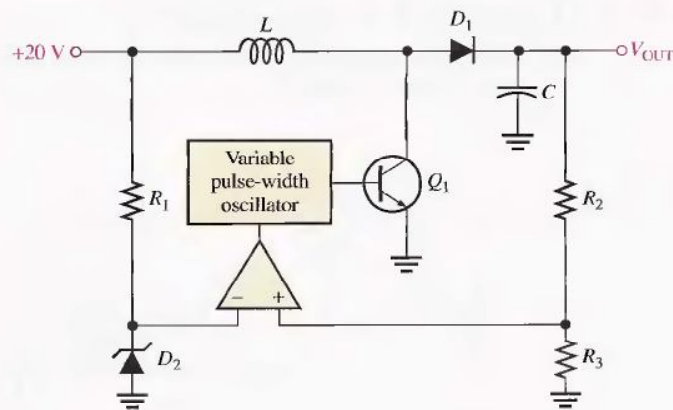
16. A basic switching regulator is shown in Figure 18-49. If the switching frequency of the transistor is 100 Hz with an off-time of 6 ms, what is the output voltage?

► FIGURE 18-49



17. What is the duty cycle of the transistor in Problem 16?
18. When does the diode D_1 in Figure 18-50 become forward-biased?

FIGURE 18-50

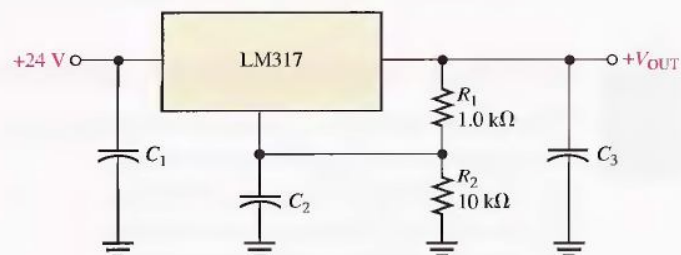


19. If the on-time of Q_1 in Figure 18-50 is decreased, does the output voltage increase or decrease?

SECTION 18-5 Integrated Circuit Voltage Regulators

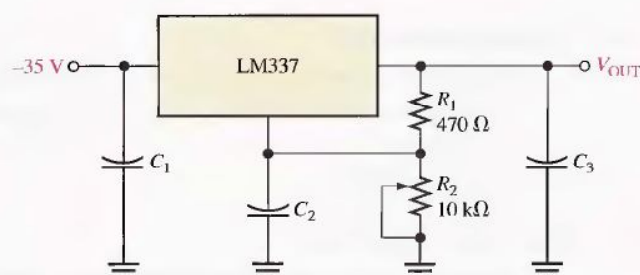
20. What is the output voltage of each of the following IC regulators?
 (a) 7806 (b) 7905.2 (c) 7818 (d) 7924
21. Determine the output voltage of the regulator in Figure 18-51. $I_{ADJ} = 50 \mu A$.

FIGURE 18-51



22. Determine the minimum and maximum output voltages for the circuit in Figure 18-52. $I_{ADJ} = 50 \mu A$.

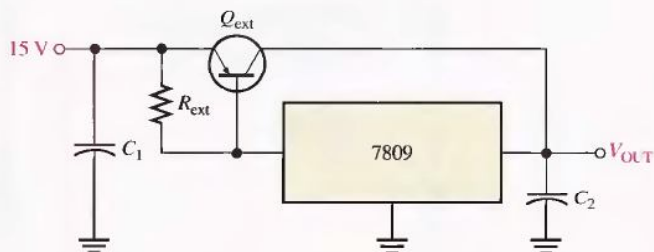
FIGURE 18-52



23. With no load connected, how much current is there through the regulator in Figure 18-51? Neglect the adjustment terminal current.
24. Select the values for the external resistors to be used in an LM317 circuit that is required to produce an output voltage of 12 V with an input of 18 V. The maximum regulator current with no load is to be 2 mA. There is no external pass transistor.

SECTION 18-6 Applications of IC Voltage Regulators

25. In the regulator circuit of Figure 18-53, determine R_{ext} if the maximum internal regulator current is to be 250 mA.

► **FIGURE 18-53**

26. Using a 7812 voltage regulator and a $10\ \Omega$ load in Figure 18-53, how much power will the external pass transistor have to dissipate? The maximum internal regulator current is set at 500 mA by R_{ext} .
27. Show how to include current limiting in the circuit of Figure 18-53. What should the value of the limiting resistor be if the external current is to be limited to 2 A?
28. Using an LM317, design a circuit that will provide a constant current of 500 mA to a load.
29. Repeat Problem 28 using a 7908.
30. If a 78S40 switching regulator is to be used to regulate a 12 V input down to a 6 V output, calculate the values of the external voltage-divider resistors.

**MULTISIM TROUBLESHOOTING PROBLEMS**

These file circuits are in the Troubleshooting Problems folder on your CD-ROM.

31. Open file TSP18-31 and determine the fault.
32. Open file TSP18-32 and determine the fault.
33. Open file TSP18-33 and determine the fault.
34. Open file TSP18-34 and determine the fault.

ANSWERS**SECTION REVIEWS****SECTION 18-1 Voltage Regulation**

1. The percentage change in the output voltage for a given change in input voltage.
2. The percentage change in output voltage for a given change in load current.
3. 1.2%; 0.06%/V
4. 1.6%; 0.0016%/mA

SECTION 18-2 Basic Series Regulators

1. Control element, error detector, sampling element, reference voltage
2. 2 V

SECTION 18-3 Basic Shunt Regulators

1. In a shunt regulator, the control element is in parallel with the load rather than in series.
2. A shunt regulator has inherent current limiting. A disadvantage is that a shunt regulator is less efficient than a series regulator.

SECTION 18-4 Basic Switching Regulators

1. Step-down, step-up, inverting
2. Switching regulators operate at a higher efficiency.
3. The duty cycle varies to regulate the output.

SECTION 18-5 Integrated Circuit Voltage Regulators

1. Input, output, and ground
2. A 7809 has a +9 V output; A 7915 has a -15 V output.
3. Input, output, adjustment
4. A two-resistor voltage divider

SECTION 18-6 Applications of IC Voltage Regulators

1. A pass transistor increases the current that can be handled.
2. Current limiting prevents excessive current and prevents damage to the regulator.
3. Thermal overload occurs when the internal power dissipation becomes excessive.

RELATED PROBLEMS FOR EXAMPLES

18-1 0.6%/V

18-2 1.12%, 0.0224%/mA

18-3 7.33 V

18-4 0.7 A

18-5 17.5 W

18-6 12.7 V

18-7 467 mA

18-8 12 W

18-9 8 Ω **CIRCUIT-ACTION QUIZ**

1. (c) 2. (a) 3. (b) 4. (a) 5. (c) 6. (a) 7. (b) 8. (b)

SELF-TEST

1. (c) 2. (d) 3. (c) 4. (b) 5. (d) 6. (a) 7. (c) 8. (a)
 9. (g) 10. (c)

19

PROGRAMMABLE ANALOG ARRAYS

INTRODUCTION

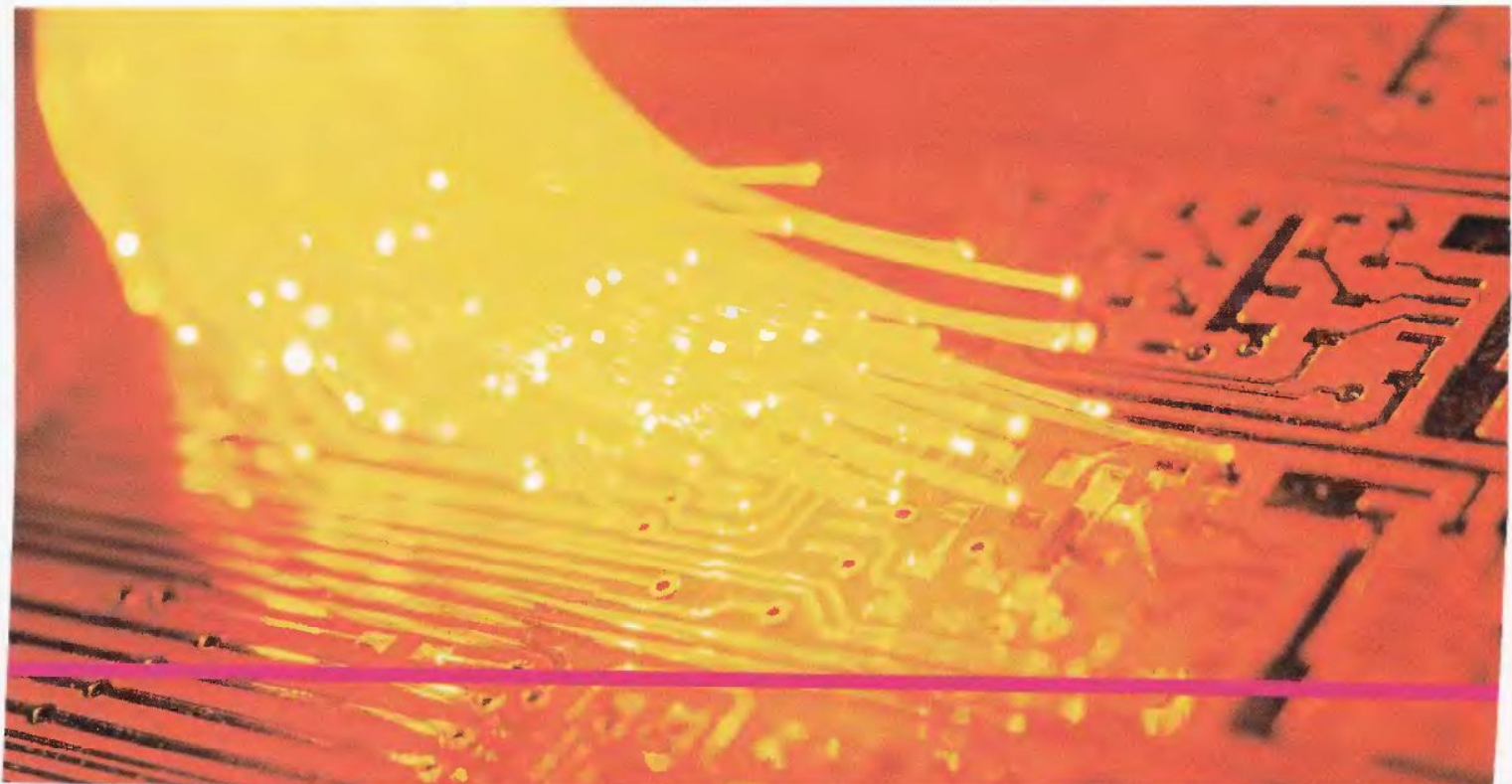
Programmable analog devices and programming are introduced in this chapter. Programmable devices have been applied in digital systems for quite some time, and they are now becoming popular for implementing analog designs.

Although programmable analog devices and software are also available from other manufacturers, selected products of Anadigm Corporation are used as examples for the topics of programmable hardware and the accompanying software in this chapter. The AnadigmDesigner2 development software is referenced and is used for illustrations. You can download a 60-day free trial version of this software at www.anadigm.com. Also, you can obtain a development kit that includes a development board with a field-programmable analog array (FPAA) installed, the interface to connect it to your

computer, and the development software. Many of the problems at the end of the chapter require the AnadigmDesigner2 software for implementing circuits up to the point of downloading them to a hardware device. If you wish to optionally download the circuits created by the software, you must have the development kit.

CHAPTER OUTLINE

- 19-1 The Field-Programmable Analog Array (FPAA)
- 19-2 Switched-Capacitor Circuits
- 19-3 A Specific FPAA
- 19-4 FPAA Programming
- System Application



CHAPTER OBJECTIVES

- Use FPAA's to implement analog circuits
- Describe the basic operation of switched-capacitor circuits
- Describe the block diagram of an AN221E04 FPAA
- Explain what is required for programming FPAA's

KEY TERMS

- FPAA
- CAB
- Switched-capacitor circuit
- Shadow RAM
- Configuration RAM
- LUT
- Development software
- CAM
- Downloading
- Dynamic reconfiguration

SYSTEM APPLICATION PREVIEW

The system application at the end of the chapter describes part of a PBX (private branch exchange), a type of private telephone network generally used by businesses. The PBX connects a certain number of telephones within a business to a smaller number of outside lines. Different PBX systems provide differing analog signals that must be conditioned. The data must be extracted from these signals and sent on for further processing. In this application, an encoding method based on AMI (alternate mark inversion) is used as an example. The portion of the system that converts the AMI signal is developed and programmed for implementation on a FPAA.

WWW. VISIT THE COMPANION WEBSITE

Study aids for this chapter are available at
<http://www.prenhall.com/floyd>

19-1 THE FIELD-PROGRAMMABLE ANALOG ARRAY (FPAA)



What an FPGA is to digital logic design, the FPAA is to analog design. The **FPAA** is a programmable integrated circuit that can be used to implement analog functions. In many applications, a programmable IC is more efficient and economical than using individual op-amps, comparators, and discrete components. Because programming can be used to change component values and interconnections, fast changes can be made in FPAAs while they are operating in a system.

After completing this section, you should be able to

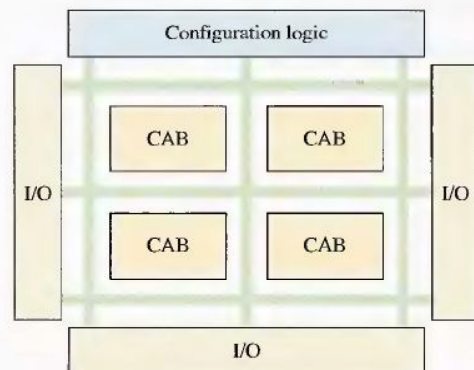
- Use FPAAs to implement analog circuits
- Describe the block diagram of a typical FPAA
- Explain a basic configurable analog block
- Program an FPAA



A typical FPAA (field-programmable analog array) includes a matrix of programmable elements, generally known as **CABs** (configurable analog blocks). The CABs are arranged within a network of programmable interconnections that allow CABs to be connected to each other as well as to input/output (I/O) interface blocks. Generally, an FPAA will contain two or more CABs and configuration logic that includes clock sources, memory, and a shift register. The software uses the configuration logic to implement a specified design. A generic block diagram for an FPAA is shown in Figure 19-1.

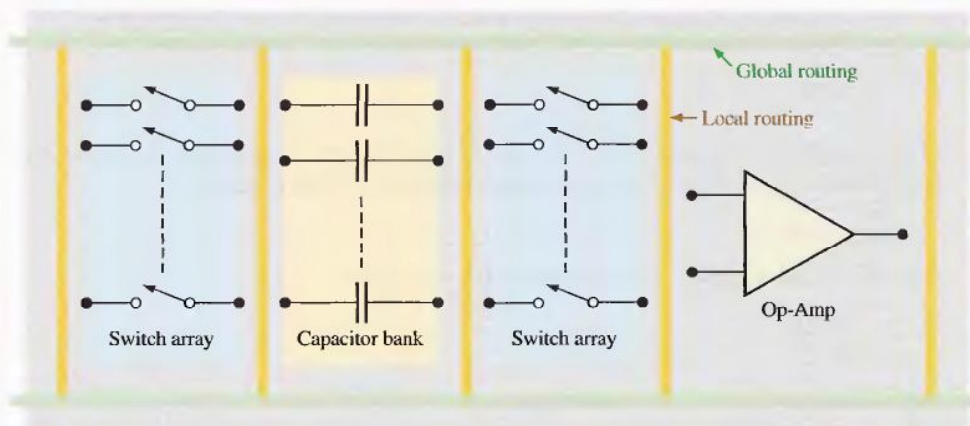
► **FIGURE 19-1**

A generic FPAA block diagram with four CABs. Programmable analog devices may contain more or fewer CABs.



The programmable features of an FPAA include the CAB, the interconnection network, and the input/output (I/O) blocks. Most FPAAs use what is known as *switched-capacitor technology* to implement various analog functions in a CAB. A typical CAB consists of one or more op-amps, a bank of capacitors, and an array of switches, as indicated in Figure 19-2. The interconnection network includes global routing, which connects to other CABs and to the outside world, and local routing, which connects within the CAB. Using these features, many analog functions (such as amplifiers, integrators, differentiators, and filters) that can be made with individual op-amps and conventional passive components (resistors and capacitors) can be implemented at less cost, in a much smaller size, and with increased reliability and component stability. In addition, the programmability makes it easy to change designs or to modify values in any given circuit or system at any time.

All FPAAs require a software development package that allows you to enter an analog circuit design on your computer, test it by simulation, and download it to the FPAA chip us-



▲ FIGURE 19-2

A simplified CAB block diagram. The switches are actually MOSFETs.

ing a standard interface. The programmable CABs and the interconnection network are controlled by on-chip clock sources, a memory, a shift register, and other logic. The software program performs the necessary operations to add the required analog functions, to make appropriate interconnections, and to properly configure the switched-capacitor networks to produce circuit values and parameters for achieving specified performance characteristics in the FPAA device.

SECTION 19-1

REVIEW

Answers are at the end of the chapter.

1. What does the acronym FPAA stand for?
2. What does the acronym CAB stand for?
3. Name the programmable features of a typical FPAA.
4. What is a common technology used to implement analog functions in a CAB?

19-2 SWITCHED-CAPACITOR CIRCUITS

Switched-capacitor circuits are used in field-programmable analog arrays to implement various analog circuits on an IC chip using only capacitors. A capacitor can be implemented on a chip more easily than can a resistor. Capacitors also offer other advantages such as no power dissipation. When a resistance is required in a circuit, a switched capacitor can be made to emulate (to imitate or act the same as) a resistor. Reprogramming switched-capacitors can readily change resistor values, and a more accurate and stable resistance can be achieved. You should have a basic understanding of switched capacitors; however, when you program an FPAA, the software shields you from all of the complex circuit details.

After completing this section, you should be able to

- Describe the basic operation of switched-capacitor circuits
- Explain how switched-capacitor circuits emulate resistors

Recall that the definition of current in terms of charge and time is expressed as

$$I = \frac{Q}{t}$$

This formula shows that current is the rate at which charge flows through a circuit. Also, recall that the definition of charge in terms of capacitance and voltage is

$$Q = CV$$

By substituting CV for Q , you can express the current as

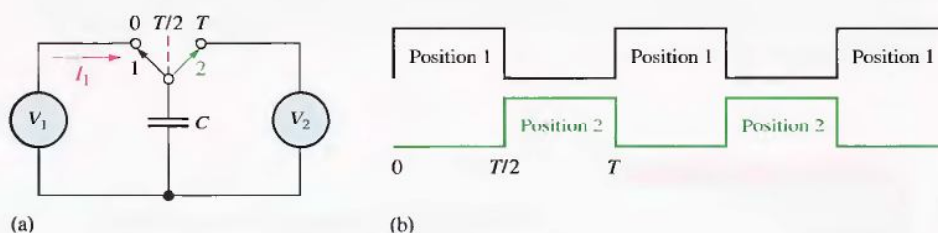
$$I = \frac{CV}{t}$$

Basic Operation

A general model of a switched-capacitor circuit, as shown in Figure 19-3(a), consists of a capacitor, two voltage sources, V_1 and V_2 , and a two-pole switch. Let's examine this circuit for a specified period of time, T . Assume that V_1 and V_2 are constant during the time period T and $V_1 > V_2$. Of particular interest is the *average* current I_1 produced by the source V_1 during the time period T .

FIGURE 19-3

Basic operation of a switched-capacitor circuit.



During the first half of the time period T , the switch is in position 1, as indicated in Figure 19-3(b). The capacitor charges very rapidly to the source voltage V_1 . Therefore, an average current I_1 due to V_1 is charging the capacitor during the interval from $t = 0$ to $t = T/2$. During the second half of the time period, the switch is in position 2, as indicated. Because $V_1 > V_2$, the capacitor rapidly discharges to the voltage V_2 . The average current produced by the source V_1 over the time period T is

$$I_{1(\text{avg})} = \frac{Q_{1(T/2)} - Q_{1(0)}}{T}$$

$Q_{1(0)}$ is the charge at $t = 0$ and $Q_{1(T/2)}$ is the charge at $t = T/2$. Therefore, $Q_{1(T/2)} - Q_{1(0)}$ is the net charge transferred while the switch is in position 1.

The capacitor voltage at $T/2$ is equal to V_1 , and the capacitor voltage at 0 or T is equal to V_2 . By substituting CV for Q in the previous equation,

$$I_{1(\text{avg})} = \frac{CV_{1(T/2)} - CV_{2(0)}}{T} = \frac{C(V_{1(T/2)} - V_{2(0)})}{T}$$

Since V_1 and V_2 are assumed to be constant during T , the average current can be expressed as

Equation 19-1

$$I_{1(\text{avg})} = \frac{C(V_1 - V_2)}{T}$$

Emulating a Resistor

In some applications where a resistance is required, a switched capacitor can be made to emulate a resistor. Figure 19-4 shows a conventional resistive circuit with two voltage sources.

From Ohm's law, the current is

$$I_1 = \frac{V_1 - V_2}{R}$$

The current $I_{1(\text{avg})}$ in the switched-capacitor circuit is equal to I_1 in the resistive circuit.

$$\frac{C(V_1 - V_2)}{T} = \frac{V_1 - V_2}{R}$$

By solving for R and canceling the $V_1 - V_2$ terms,

$$R = \frac{T(V_1 - V_2)}{C(V_1 - V_2)}$$

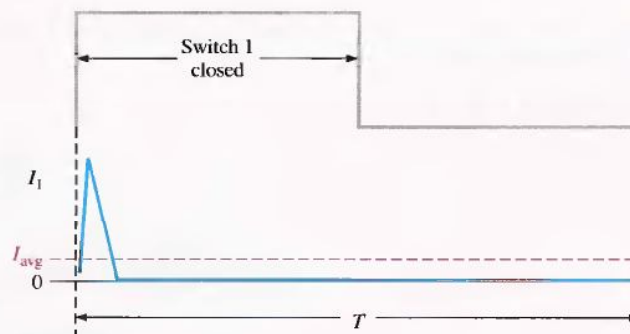
$$R = \frac{T}{C}$$

As you can see, a switched-capacitor circuit can emulate a resistor with a value determined by the time period T and the capacitance C . Remember that the two-pole switch is in each position for one-half of the time period T and that you can vary T by varying the frequency at which the switches are operated.

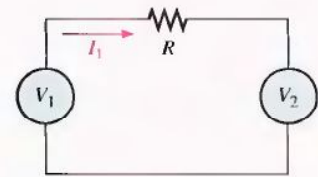
In an FPAA, the switching frequency is a programmable parameter for each emulated resistor and is selected to achieve a precise resistor value. Since $T = 1/f$, the resistance in terms of frequency is

$$R = \frac{1}{fC}$$

The Charging Current Figure 19-5 illustrates the charging current in a switched capacitor. At the beginning of T , the capacitor rapidly charges, resulting in a short spike of current that charges the capacitor to V_1 . During the remaining portion of T , the current produced by V_1 is zero. The average current for the time period T depends only on the total charge that is transferred and on the time period T . If T is reduced, the average current increases because the time is shorter for a given amount of charge. If T is increased, the average current decreases because the time is longer for a given amount of charge.



For a given value of T , if the value of C is increased, more charge is transferred when the switch goes to position 1, resulting in a greater average current. If the value of C is reduced, less charge is transferred when the switch goes to position 1, resulting in less average



▲ **FIGURE 19-4**
Conventional resistive circuit.

Equation 19-2

Equation 19-3

▲ **FIGURE 19-5**
Charging current in a switched capacitor.

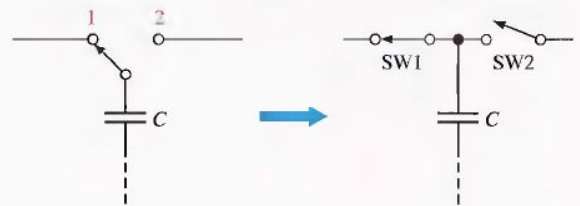
current. For a given voltage, an increase in average current effectively corresponds to a decrease in resistance and a decrease in average current effectively corresponds to an increase in resistance. This discussion has shown that the effective emulated resistance is directly related to T and inversely related to C , as was stated in Equation 19-2.

Practical Switches

The two-pole switch that has been used to illustrate the basic concept of a switched-capacitor circuit is an impractical form in terms of its implementation in an FPAA. Figure 19-6 shows how the simple two-pole switch can be replaced by two single-pole switches. You can see that when SW1 is closed and SW2 is open, it is equivalent to the two-pole switch being in position 1. When SW1 is open and SW2 is closed, it is equivalent to the two-pole switch being in position 2.

► **FIGURE 19-6**

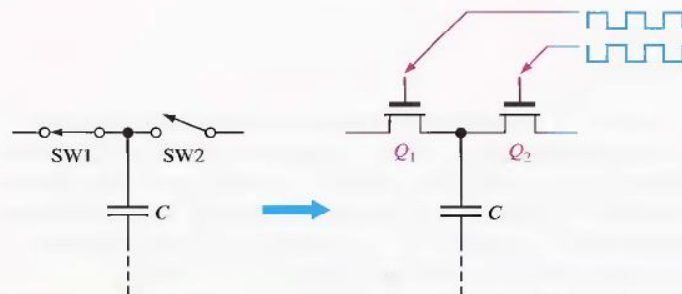
Switch equivalents.



As you know, switches in electronic circuits are implemented with transistors. Typically, the switch array implemented in an FPAA consists of MOSFET switches. A switched-capacitor circuit is shown in Figure 19-7 with MOSFETs acting as the switches. Their *on* and *off* times are controlled by timing signals with frequencies that are programmable. The two timing signals that turn the MOSFETs on and off are square waves that are 180° out of phase so that when one transistor is *on* the other is *off* and vice versa with no overlap.

► **FIGURE 19-7**

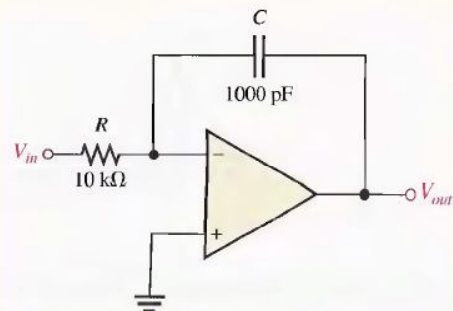
A switched-capacitor with MOSFET switches.



EXAMPLE 19-1

Replace the input resistor in the integrator of Figure 19-8 with a switched-capacitor and show the resulting circuit.

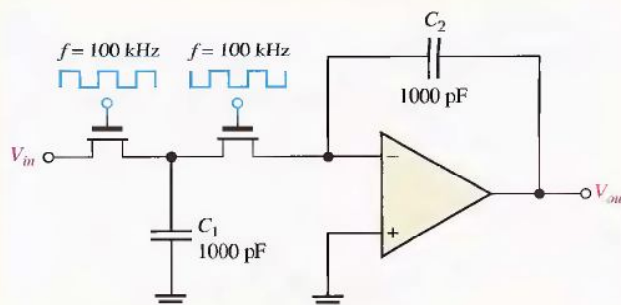
► **FIGURE 19-8**



Solution An integrator with a switched-capacitor circuit that emulates the resistor is shown in Figure 19-9.

► **FIGURE 19-9**

Switched-capacitor integrator equivalent to the circuit in Figure 19-8.



The values shown in Figure 19-9 are determined as follows. Assume that the switched-capacitor value is 1000 pF. You want the switched capacitor to emulate a 10 k Ω resistor by effectively providing the same average current as the actual resistor would. Using the formula $R = T/C$,

$$T = RC = (10 \text{ k}\Omega)(1000 \text{ pF}) = 10 \mu\text{s}$$

This means that each switch must be operated at a frequency of

$$f = \frac{1}{T} = \frac{1}{10 \mu\text{s}} = 100 \text{ kHz}$$

The duty cycle should be 50% so that the switch is in each position half of the period. Two non-overlapping 100 kHz, 50% duty cycle voltages that are 180° out-of-phase with each other are applied to the transistor switches in Figure 19-9.

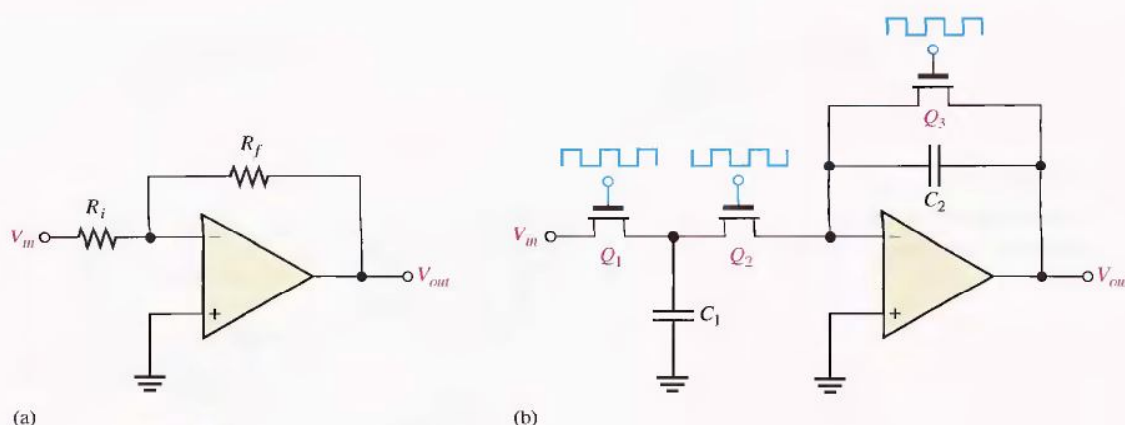
Related Problem* At what frequency must the switches be operated in Figure 19-9 to emulate a 5.6 k Ω resistor?

* Answer is at the end of the chapter.

Emulating Feedback Resistors

You have seen in the preceding discussion and example how the input resistor to an op-amp circuit can be emulated with a switched-capacitor circuit. However, feedback resistors, such as used in differentiators, inverting and noninverting amplifiers, and certain types of filters require a variation in approach.

The switched-capacitor implementation for the input resistor used in the integrator of Figure 19-9 is impractical for emulating a feedback resistor such as shown in the op-amp in Figure 19-10(a). Because the two transistor switches are never on at the same time, the feedback path would never be closed and proper operation would be prevented. To avoid this, the switched-capacitor configuration for the feedback loop in the amplifier in Figure 19-10(b) can be used. Q_1 and Q_3 are on at the same time. Q_1 allows C_1 to charge to the input voltage and C_2 discharges through Q_3 . When Q_2 turns on, the



▲ FIGURE 19-10

Amplifier with switched-capacitor emulation of input and feedback resistors.

sampled input voltage stored on C_1 is applied to the input of the op-amp and charges Q_3 . The voltage gain is

$$A_v = -\frac{\left(\frac{1}{fC_2}\right)}{\left(\frac{1}{fC_1}\right)} = -\frac{\left(\frac{1}{C_2}\right)}{\left(\frac{1}{C_1}\right)}$$

Equation 19-4

$$A_v = -\frac{C_1}{C_2}$$

SECTION 19-2 REVIEW

1. How are switched-capacitor circuits applied in FPAA's?
2. How does a switched capacitor emulate a resistor?
3. What factors determine the resistance value that a given switched-capacitor circuit can emulate?
4. In a practical implementation, what devices are used for switches?

19-3 A SPECIFIC FPAA

In this section, we look at the Analog Devices AN221E04 FPAA as an example of a typical programmable analog array. FPAAs generally can be reprogrammed many times. This particular device is reprogrammable and can be dynamically configured, which means that it can be reprogrammed after being installed and while operating in a system.

After completing this section, you should be able to

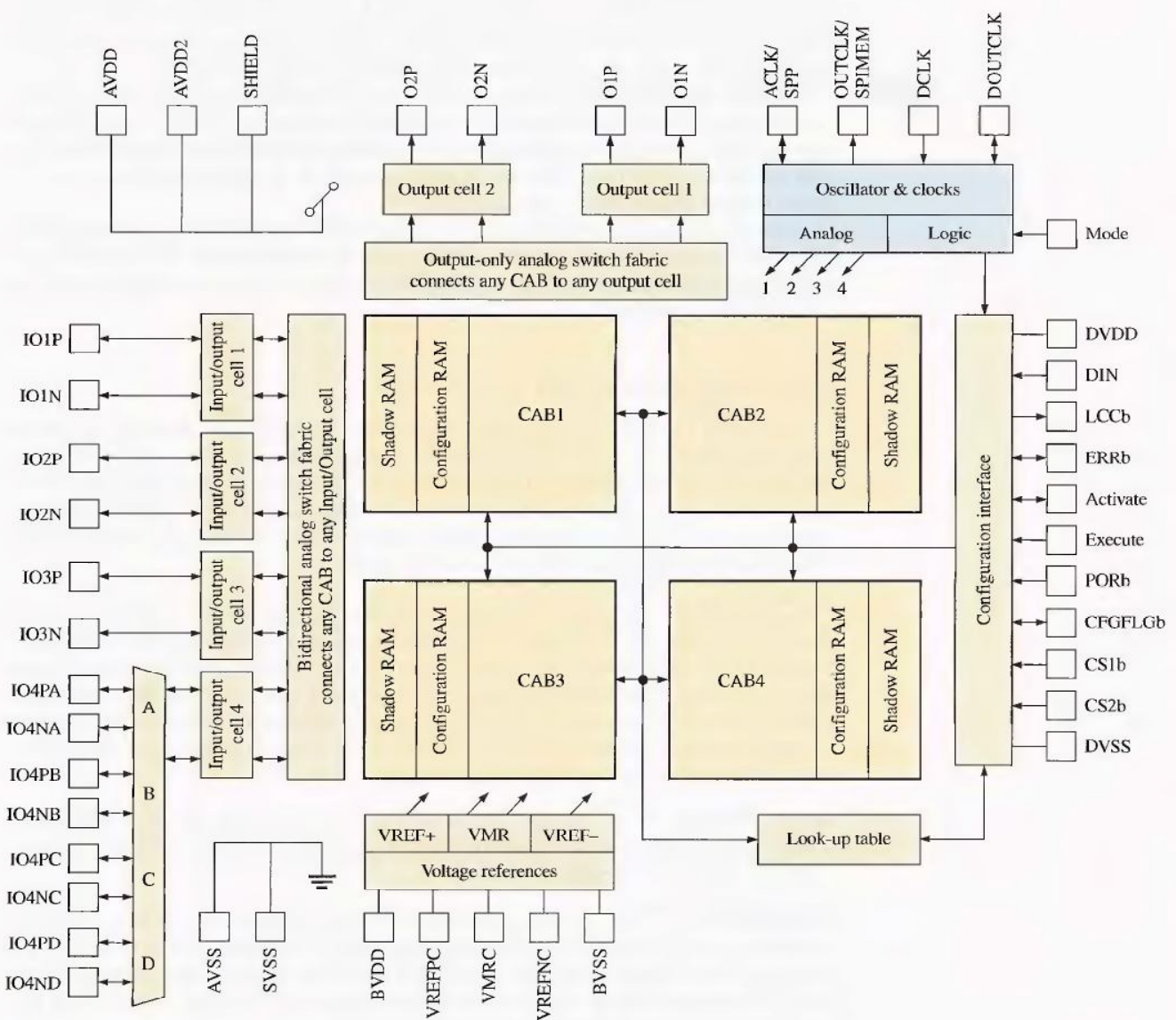
- Describe the block diagram of an AN221E04 FPAA
- Describe the CAB in an AN221E04

Overview of the AN221E04

A typical package and block diagram for an AN221E04 FPAA are shown in Figure 19–11.



(a)



(b)

▲ FIGURE 19–11

Device package and block diagram of the AN221E04.

This device has four CABs arranged in a 2×2 matrix and includes the associated logic and other resources for initial programming and reconfiguration.

When you program the FPAA, the data goes into the on-chip random-access memories (RAMs) associated with each CAB via the configuration interface. These memories allow reconfiguration data to be loaded while the old configuration is active and running. The **shadow RAM** stores the new configuration data without disturbing the current configuration until the proper time for it to be transferred into the **configuration RAM**, which stores the current configuration data. This permits any changes or adjustments in circuit design to be accomplished while the FPAA is operating in a system without disturbing the system operation. This is called *dynamic reconfiguration*.

Configuration data can be generated from a computer running the development software when the FPAA is initially programmed. Data for configuring the device can also be generated from an external EPROM that is storing the configuration program, or reconfiguration can be controlled by a microprocessor, called a **host processor**, embedded in the system in which the FPAA is operating. The FPAA device can generate its own clock for internal timing, or it can accept an external clock signal. DC voltages can be generated internally for use in certain types of circuits that require reference voltages.

The **look-up table (LUT)** in the FPAA is a type of memory that stores data for certain predetermined configuration functions. It contains storage space for 256 bytes of data (a **byte** is 8 bits). Each byte of storage space has a specific address that uniquely defines it. An 8-bit address code can be produced by a special counter or by the SAR-ADC (successive-approximation register-ADC) logic in a CAB.

Analog input signals are connected to the device with the configurable input/output (I/O) cells. Output signals can also be routed through the input/output cells. An I/O cell can accept a differential or common-mode input signal and can contain a programmable filter and amplifiers for improving input signal quality.

The Configurable Analog Block (CAB)

As you saw in Figure 19–11, there are four CABs in the AN221E04 device. A circuit design is programmed into the CABs using development software with a library of analog functions, such as integrators, differentiators, filters, comparators, and other types of circuits. The development software will be introduced in Section 19–4. A CAB block diagram is shown in Figure 19–12. Notice that there are two op-amps and one comparator available in addition to the capacitor bank and switch matrices.

The Control Logic The control logic in a CAB transfers data from the outside world into the shadow SRAM (static random-access memory) and then copies it into the configuration SRAM. As previously mentioned, data for updating the configuration SRAM can be loaded into the shadow SRAM while the FPAA is operating in a system without affecting the operation. The data in the shadow SRAM can then be moved to the configuration SRAM at an appropriate time to reprogram the device or modify specified parameters. This is sometimes referred to as “on-the-fly” reprogramming.

Switch Matrices There are two arrays of switches, controlled by the configuration SRAM, that are used for circuit connections, setting capacitor values, switched-capacitor operation, and input selection.

Capacitor Banks There are many small equally sized capacitors that can be programmed for relative values of from 0 to 255 units of capacitance. Capacitors can be programmed in series to achieve lower capacitance values or in parallel to achieve larger capacitance values. The capacitors can be connected for fixed values, or they can be connected and programmed as switched capacitors to emulate resistors.

When used as switched capacitors, non-overlapping (NOL) clock signals are required as previously discussed. These non-overlapping clocks are produced by the NOL clock generator.

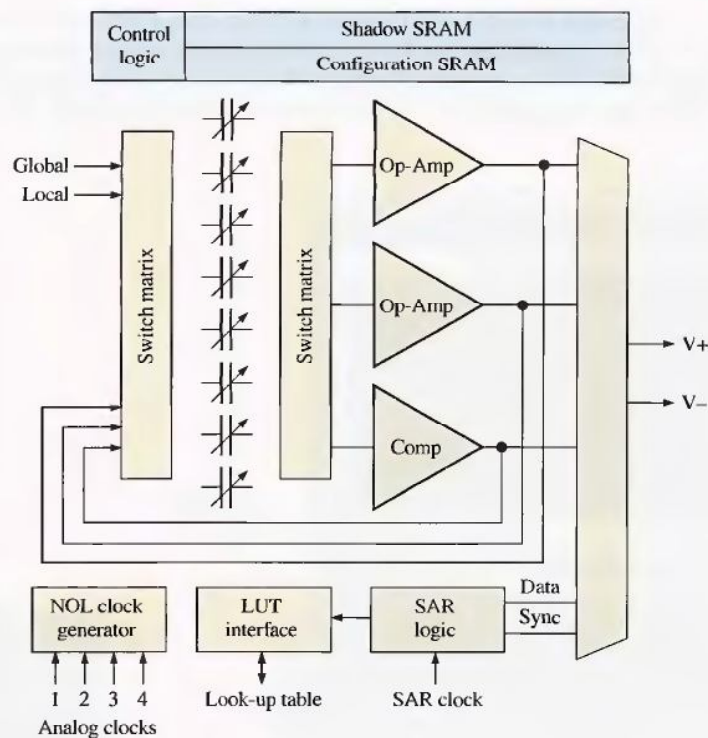


FIGURE 19-12

One CAB in an AN221E04 FPAA.

LUT Interface The LUT (look-up table) interface in each CAB provides access to the look-up table, which was described earlier. The SAR logic is a successive-approximation register used as an analog-to-digital converter (ADC). The address codes generated by the SAR-ADC logic are used to access data stored in the LUT that can be used for modification of analog input signals and other functions.

SECTION 19-3 REVIEW

1. What are the major elements of a CAB in an AN221E04 FPAA?
2. What are the two RAMs in an AN221E04?
3. State the purposes of a switch matrix.
4. Describe one purpose of the non-overlapping (NOL) clock generator?

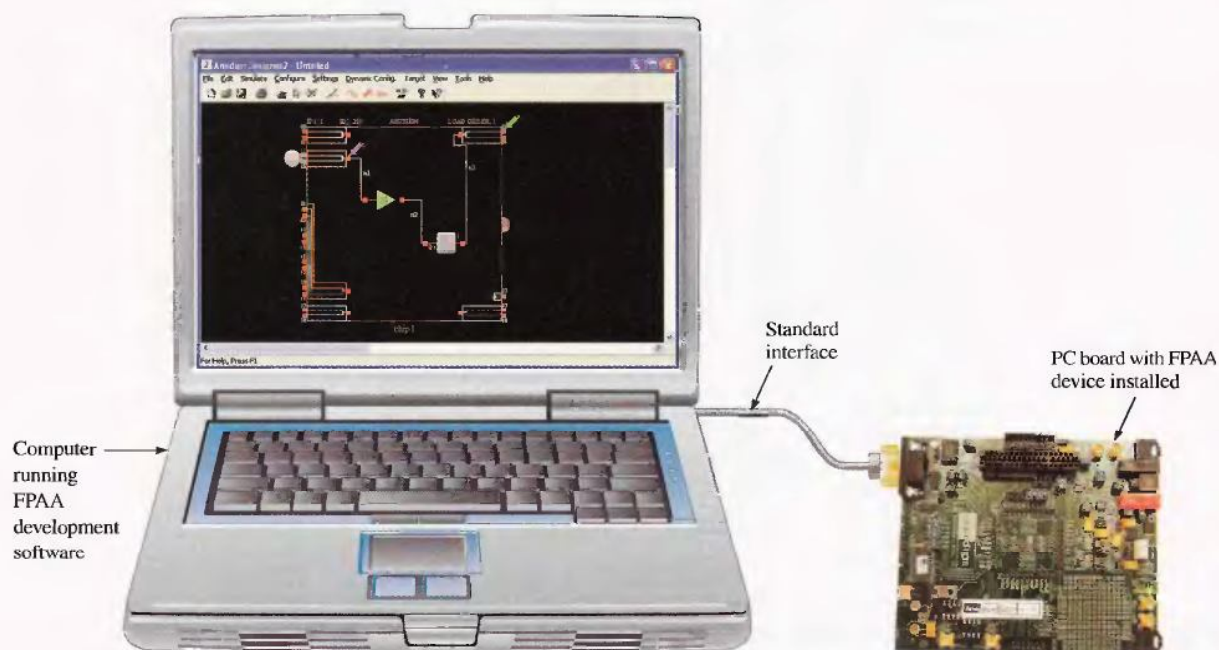
19-4 FPAA PROGRAMMING

FPAAs are programmed using development software that provides for implementing analog circuit designs on a chip and also shields you from the details of the circuit implementation. An FPAA can be originally programmed or reprogrammed statically on an evaluation or development board. Once the design has been completed and tested on the evaluation board, it can then be dynamically programmed into FPAAs installed on a system board. In this section, we look at the process of configuring an FPAA.

After completing this section, you should be able to

- Explain what is required for programming FPAAs
- Discuss the general sequence of steps in FPAA programming

The general setup for programming a circuit design into an FPAA includes a computer running the development software, a pc board with a standard interface to a computer port, and the FPAA device installed on the pc board (usually called a development or an evaluation board). A representation of this setup is shown in Figure 19–13.



▲ FIGURE 19–13

Simplified illustration of the setup for programming an FPAA.

Development Software



Development software provides for entering a circuit design on the computer, simulating the design to make sure that it operates as expected, and downloading the design to the FPAA chip.

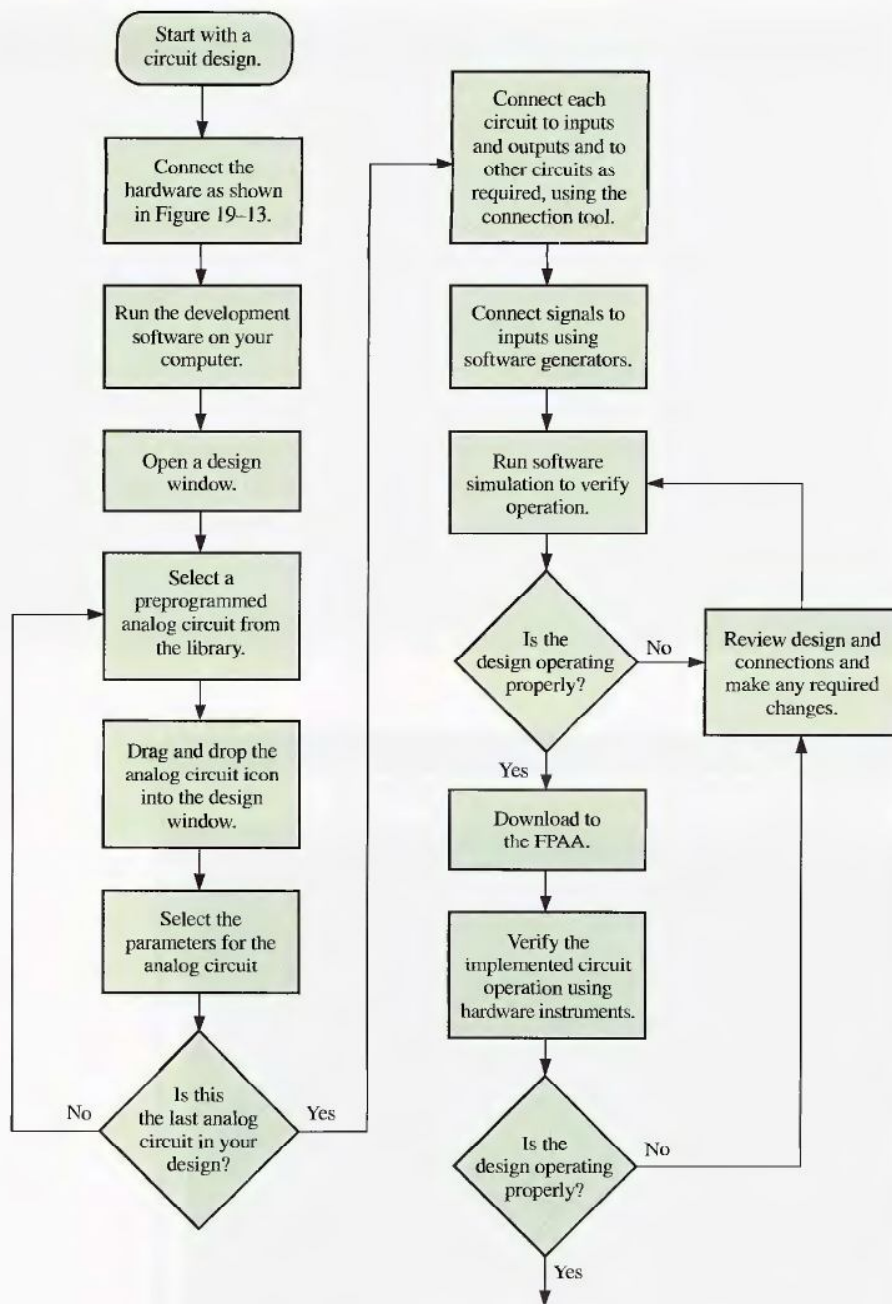
Using the software, you can select from a library of analog circuits, then drag and drop the selected ones onto the screen. Once the circuits are on the screen, certain parameters can be set. For example, you can set the gain of an amplifier, the critical frequency of a filter, the output rate of change of an integrator, and so on. The circuits can then be connected to inputs and outputs and to each other to create an on-screen circuit diagram. Once the circuit is tested, you can then download it to the chip. A flow chart showing the general programming procedure is given in Figure 19–14.

Occasionally, when a circuit design is downloaded to the FPAA, the operation may vary slightly from that of the software simulation. In this event, an FPAA chip can be reprogrammed as many times as needed in order to tweak or adjust the design to achieve the precise hardware operation that is required.

Programming with a Specific Development Software



An excellent example of FPAA development software is the AnadigmDesigner2. The AnadigmDesigner2 software provides for the selection, placement, wiring, and simulation of one or more subcircuits called CAMs. The CAMs (configurable analog modules) are the “building blocks” for analog designs and are preconstructed analog functions that can be adjusted for desired parameter values.



◀ **FIGURE 19-14**

Flow chart for general programming of an FPAA.

A partial list of available CAMs is given in Table 19-1. For each CAM, the parameters can be programmed or reprogrammed for desired performance. For example, for the bi-quadratic filter CAM you can set the gain, critical frequency, and Q . Some CAMs are single function, such as the integrator; some are multiple function, such as the biquadratic filter where you can select low-pass, high-pass, band-pass, or band-stop versions.

Begin with a blank design window as shown in Figure 19-15. CAMs will be selected and placed in this window and connected. At any time, you can start over with a blank design window by selecting *New* from the File menu or by deleting a CAM and connections. Only a brief description of each step is given. For more details on any steps, refer to the website at www.anadigm.com to download appropriate literature. We will use a very simple single-CAM circuit to illustrate the steps.

TABLE 19-1

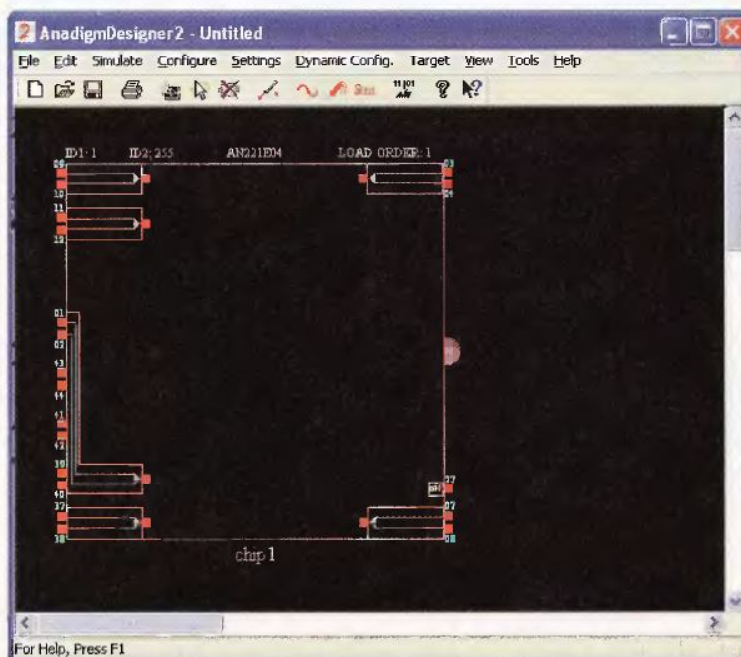
Partial list of the CAMs available in the AnadigmDesigner2 software.

CONFIGURABLE ANALOG MODULES (CAMs)

Analog-to-digital converter	Integrator
Bilinear filter	Inverting gain stage
Biquadratic filter	Inverting sum stage
DC voltage source	Multiplier
Differential comparator	Periodic waveform generator
Differentiator	Rectifier with low-pass filter
Divider	Sample-and-hold
Gain stage with output voltage limiting	Sine wave oscillator
Gain stage with polarity control	Square root circuit
Gain stage with switchable inputs	Sum/difference stage with low-pass filter
Half-cycle gain stage	Voltage-controlled variable gain stage
Half-cycle inverting gain stage	Voltage transfer function
Half-cycle inverting rectifier	
Half-cycle rectifier	

FIGURE 19-15

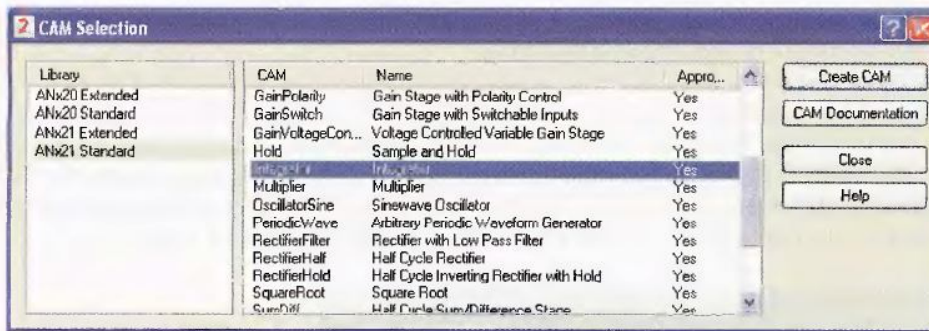
Blank design window.



The next step is to select a CAM from the CAM Selection Dialog Box, which is opened by clicking on the symbol in the tool bar. In this case, we have selected the integrator as shown in Figure 19-16.

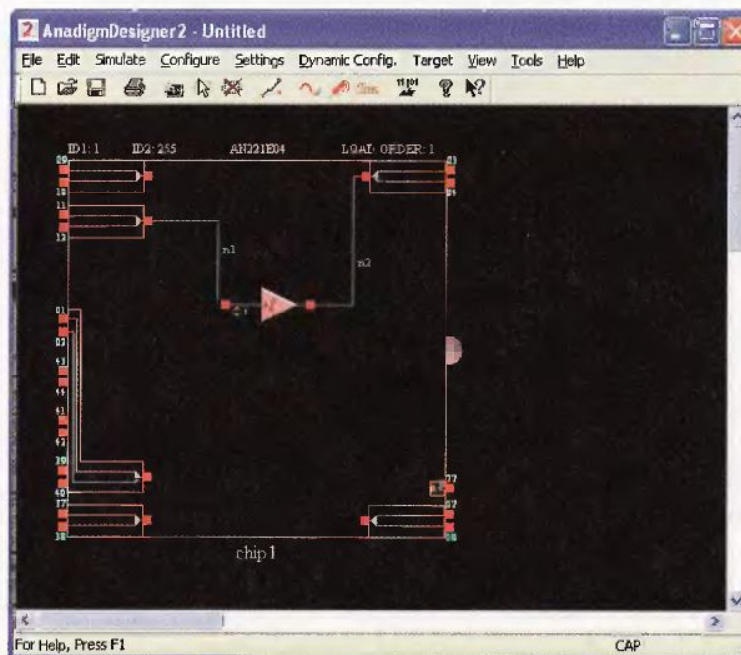
Next, drag the selected CAM icon and drop it into the design window. Using the connection tool, “wire” the CAM as required. In this case, the integrator is simply connected to an input and an output, as indicated in Figure 19-17.

Once the CAM is selected and before it is wired, the Parameters box appears, as shown in Figure 19-18. The number of parameters that you can set depends on the type of CAM.



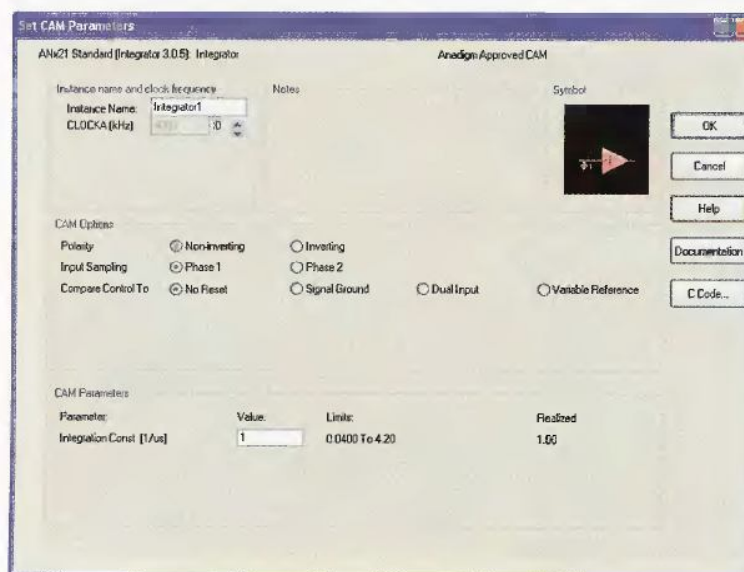
◀ FIGURE 19-16

Dialog box for selection of configurable analog modules (CAMs).



◀ FIGURE 19-17

The integrator CAM is dropped into the design window and connected.



◀ FIGURE 19-18

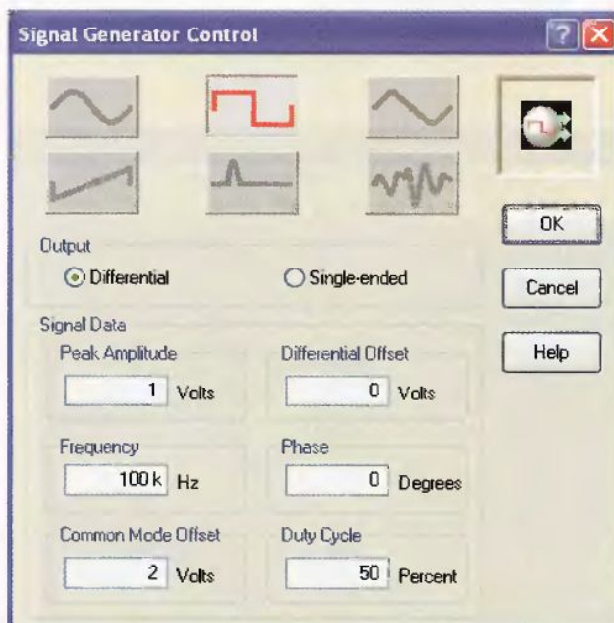
Dialog box for setting CAM parameters.

In this case, the integration constant is the only parameter to be determined. Also, you can make the integrator inverting or noninverting.

The circuit is now installed and connected in the design window, and you have selected the CAM parameter(s). Now, you should verify that the circuit operates properly by running a simulation. First, select the signal generator and place the icon at the input pin. Click on the icon to bring up the parameter window, select the appropriate function, and set the values. In this example, the pulse output has been selected, the frequency has been set to 100 kHz, the peak value to 1 V, and the duty cycle to 50%, as shown in Figure 19-19.

► **FIGURE 19-19**

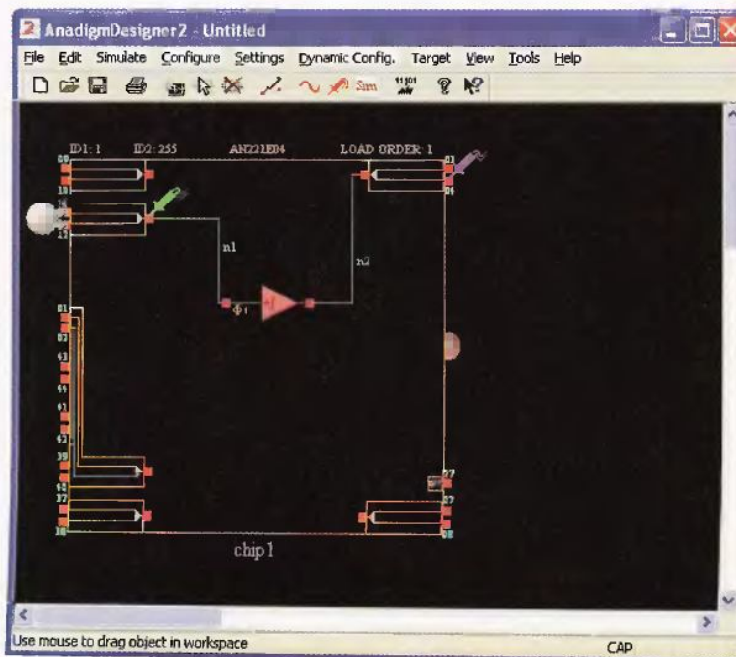
Signal generator parameter window.



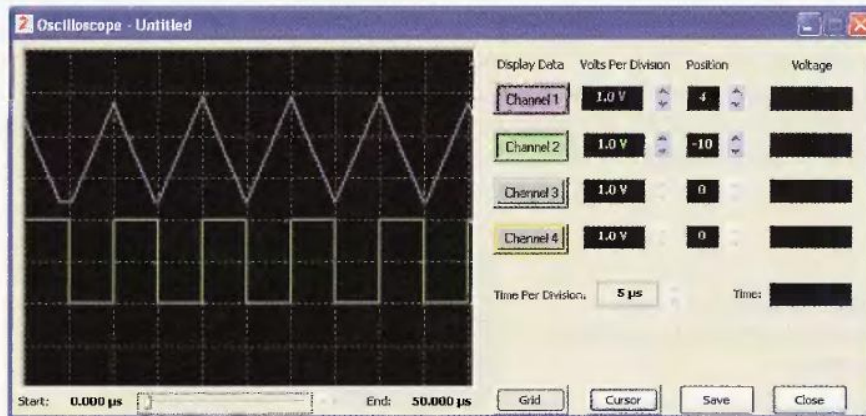
Finally, select the oscilloscope probe icon and place it on the input. Select it again and place another probe on the output, as shown in Figure 19-20. Up to four probes can be placed on wires, CAM inputs or outputs, or any input or output cell.

► **FIGURE 19-20**

Source connected and oscilloscope probes placed on input and output of circuit for simulation.



Begin the simulation and observe the result on the oscilloscope. In this example, the input is the square wave, and the output is the triangular wave, as shown in Figure 19–21.



◀ **FIGURE 19–21**

Oscilloscope display verifies circuit operation.

Downloading the Circuit to the FPAA Assuming that an evaluation board (one type is shown in Figure 19–22) is connected to the serial port of the computer, you can download the design to the FPAA installed on the board. **Downloading** is the process of putting the software design into the FPAA chip and is accomplished by selecting the menu item *Configure > Write the configuration data to serial port*. It takes only about two seconds. After the download, the circuit is implemented in the chip and can be tested by connecting an actual signal generator and oscilloscope to the appropriate pins on the board.



◀ **FIGURE 19–22**

An evaluation board with an FPAA installed.

Hosted Operation of an FPAA

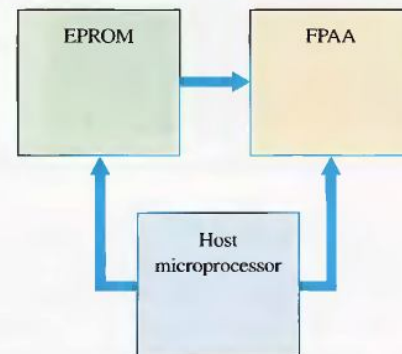
After an analog circuit design has been perfected using a development or evaluation board, the design configuration data file can be loaded into an EPROM that is installed with an FPAA in a system. The FPAA can then initially configure itself from the EPROM on

power-up or system reset. This is a form of static configuration because the FPAA programming must start from scratch when power is first applied or when the system is reset, not while it is actively performing its designed operation.

A major advantage of an FPAA is that it can also be dynamically reconfigured. **Dynamic reconfiguration** means that a design modification or a completely new design can be downloaded to an FPAA while it is operating in a system without the need to power down or to reset the system. This is known as “on-the-fly” reconfiguration and is accomplished by connecting the FPAA to a companion or host microprocessor, as shown by a simplified block diagram in Figure 19-23.

► **FIGURE 19-23**

Simplified diagram of a host processor and EPROM connected to an FPAA.



With the host processor, both static and dynamic reconfiguration can be accomplished. To reconfigure an FPAA statically, a system reset sequence is required prior to the design data file being transferred by the host processor to the FPAA. To reconfigure an FPAA dynamically, the design data file can be transferred “on-the-fly” in a single clock cycle without resetting the system. Dynamic reconfiguration is especially useful in applications where certain parameters in the initial design must be adjusted or updated without interrupting the system operation.

AnadigmDesigner2 software uses C code to create and download data “on-the-fly” from the EPROM to the FPAA under the control of the host processor in response to changing requirements for the analog circuit in the FPAA. Each configurable analog module (CAM) has associated C code functions that are used to manipulate its programmable parameters. One example of a C code application is in the case of an adjustable filter where the number and type of filter stages is fixed, but the critical frequency, Q , and gain require periodic adjustment “on-the-fly.”

SECTION 19-4 REVIEW

1. State the purposes of FPAA development software.
2. What is a CAM?
3. What does downloading accomplish in the FPAA programming process?
4. What is the major difference between static and dynamic reconfiguration?
5. What does the term “on-the-fly” mean?



SYSTEM APPLICATION

A PBX (private branch exchange) is a private telephone network generally used by businesses. The PBX connects a certain number of telephones within a business to a smaller number of outside lines. For example, there may be four outside lines for twenty telephones. The PBX is much less expensive than connecting a separate outside telephone line to every telephone in the organization. Also, to call someone else on the same PBX system requires dialing fewer digits (typically three or

four). A variation of the PBX is the *centrex*, which is a type of PBX with the switching equipment located at the telephone exchange instead of at a company's premises.

Different PBX systems provide various types of signals that must be conditioned. The data must be extracted from these signals and sent on for further processing. FPAA's can be used to provide the analog signal processing portion of a PBX's operation.

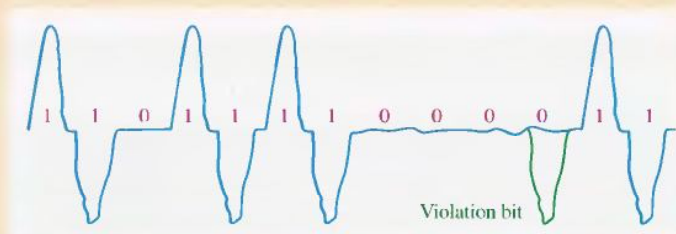
Signal Encoding

In this application, an encoding method based on AMI (alternate mark inversion) is used. AMI uses three voltage levels to represent digital data, which consists of 1s and 0s. In an AMI signal, either a positive or a negative signal voltage represents a 1 and zero signal voltage represents a 0. The alternate polarity coding is used because it prevents the buildup of a dc voltage level down the telephone cable. An example of an AMI signal and the bit stream that it represents is shown by the blue waveform in Figure 19-24.

A long string of 0s in the synchronized AMI signal produces no transitions, and can prevent the clock from being reliably recovered by the PLL at the receiving end, thus causing loss of synchronization and resulting in errors. To overcome this problem, new encoding methods have been developed. One of these methods is called *high-density bipolar order 3* (HDB3) and is based on AMI but avoids the problem of losing synchronization created when long strings of 0s occur. HDB3 is the same as AMI except that a sequence of four consecutive 0s are encoded using a *violation bit*, which has the same polarity as the last 1, in order to introduce a transition for maintaining synchronization, as shown by the green pulse in Figure 19-24.

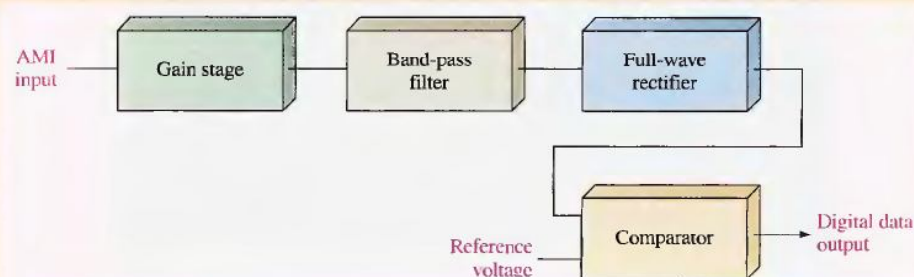
Conversion of an AMI Signal

An AMI (or HDB3) signal must be converted to a series of single-polarity pulses that can be processed in the PBX. A block diagram for converting an AMI signal to single-polarity data is shown in Figure 19-25.



▲ FIGURE 19-24

Example of an AMI (alternate mark inversion) signal.



▲ FIGURE 19-25

Basic block diagram of AMI conversion.

This circuit has an amplifier with gain (gain stage) at the input. The band-pass filter is used to remove high-frequency noise and the 60 Hz component present in the system. The signal out of the filter goes to the full-wave rectifier to make all the pulses positive. The signal then goes to one of the comparator inputs. Every time the signal out of the rectifier crosses a threshold established by a reference voltage, the comparator produces a positive pulse, representing a 1. When the rectifier output is zero, the comparator output is at its low level, representing a 0.

The FPAA Implementation

The circuit represented by the block diagram in Figure 19-25 is implemented with CAMs, as shown in Figure 19-26. The amplifier is an inverting gain stage; the filter is a biquad filter selected for the band-pass mode; the rectifier is a full-wave rectifier with low-pass filter; and the comparator has a variable voltage

reference on the inverting input. The output cell is configured for a digital output to produce a sharp digital signal for processing by other circuits.

To simulate the operation, an AMI input waveform must be captured into a data file with time/amplitude pairs so that the software signal generator can be used. There is a data file selection button on the AnadigmDesigner2 signal generator dialog box. Using the data file waveform generator, you can produce any waveform you need. Each record in the data file consists of ASCII codes representing the time and amplitude of a waveform at a point. When many of these time/amplitude pairs are connected by the simulator, a piecewise linear waveform is generated. Spreadsheet programs are useful in creating piecewise linear signal data files, but this topic is beyond our scope.

A PBX signal can originate from different switch manufacturers, so the signal characteristic that the FPAA imple-

mentation must handle, usually signal amplitude and shape, can vary. The gain stage and the reference voltage can be reprogrammed to accommodate these variations in signal characteristics. The frequency used in PBXs is constant so the filter does not normally have to be reprogrammed. Reconfiguration allows a single design to be used to interface with a variety of PBX switches.

Simulate the Design

Use a 20 kHz, 2 V triangular wave input signal to check the circuit. Place probes as shown in Figure 19-27 and run the simulation. Although the input is not an AMI type signal, the alternating triangular wave shows that the rectifier output is triggering the comparator at a reference voltage of 1 V to produce a digital output, as shown in Figure 19-28. The color of each signal corresponds to the color of the probe to identify the points being measured.

Using the AnadigmDesigner2 software, run this simulation.

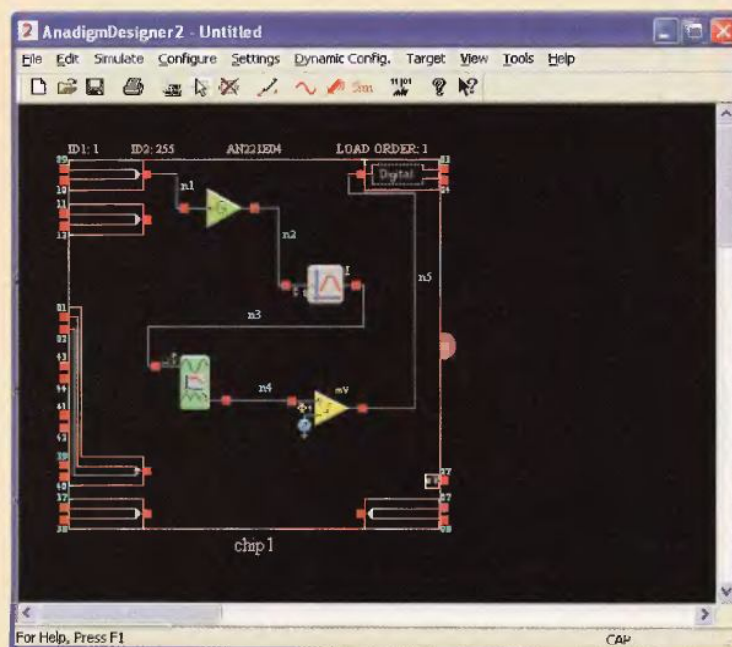


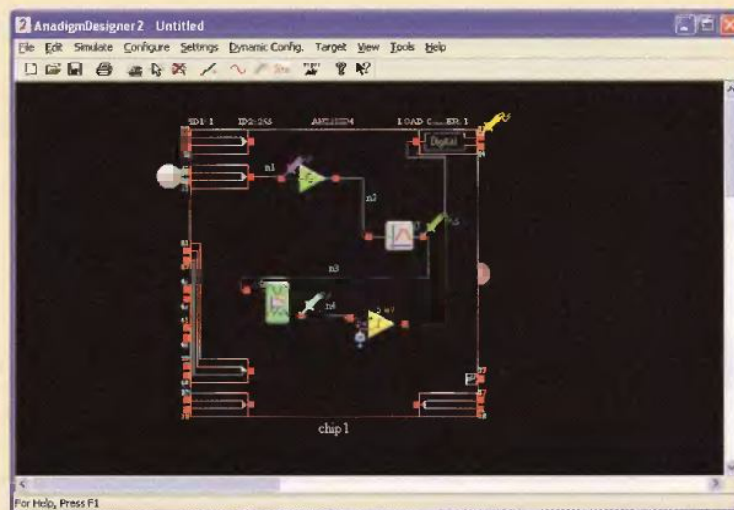
FIGURE 19-26

Implementation of the block diagram in Figure 19-25.

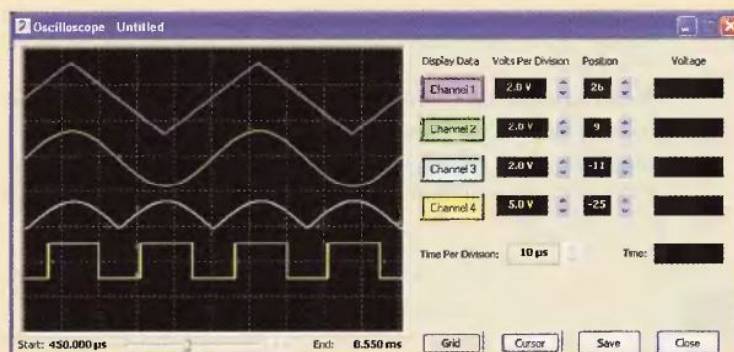
- Change the comparator reference voltage to 0.5 V and observe the output.

- Change the comparator reference voltage to 1.5 V and observe the output.

- Return the reference voltage to 1 V, change the gain of the amplifier to 2, and observe the output.



▲ FIGURE 19-27



▲ FIGURE 19-28

Waveforms for the circuit in Figure 19-27.

CHAPTER SUMMARY

- An FPAA consists of two or more configurable analog blocks.
- Most FPAAs used switched-capacitor circuits.
- A switched-capacitor circuit is based on charge flow and can emulate a resistor with a value determined by the capacitance value and the frequency at which it is switched.
- The AN221E04 FPAA has four configurable analog blocks (CABs) arranged in a 2×2 matrix.
- An FPAA can be programmed or configured statically while installed on a development or evaluation board or dynamically while operating in a system.
- Development software provides for entering a circuit design using a computer, simulating the design to make sure that it operates as expected, and downloading the design to an FPAA device.
- The setup for statically programming an FPAA requires a computer running the development software, an FPAA device installed on a development or evaluation board, and a standard between the computer port and the board.
- Typical development software provides configurable analog modules that can be dragged and dropped into a design window on the computer screen and then connected.
- Configurable analog modules (CAMs) include standard analog functions such as filters, gain amplifiers, rectifiers, comparators, summing amplifiers, integrators, differentiators, and so on with programmable parameters.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

CAB Configurable analog block; one of the programmable elements in an FPAA, generally consisting of one or more op-amps, a switch matrix, and a capacitor bank.

CAM Configurable analog module; a predesigned analog circuit for which some of its parameters can be selectively programmed.

Configuration RAM A random-access memory used in FPAAs for storing configuration data from the shadow RAM immediately prior to reconfiguring the FPAA.

Development software A software that is used for entering a circuit design on the computer, simulating the design, and downloading the design to the FPAA device.

Downloading The process of implementing the software description of a circuit in an FPAA.

Dynamic reconfiguration The process of downloading a design modification or new design in an FPAA while it is operating in a system without the need to power down or reset the system; also known as on-the-fly reprogramming.

FPAA Field-programmable analog array; an integrated circuit that can be programmed for implementation of an analog circuit design.

LUT Look-up table; a type of memory that stores preprogrammed data for use in the reconfiguration of an FPAA.

Switched-capacitor circuit A combination of a capacitor and transistor switches used in programmable analog devices to emulate resistors.

Shadow RAM A random-access memory used in FPAAs for temporarily holding data while the device is operating and before it is loaded into the configuration RAM for reprogramming.

KEY FORMULAS

$$19-1 \quad I_{I(\text{avg})} = \frac{C(V_1 - V_2)}{T}$$

$$19-2 \quad R = \frac{T}{C}$$

$$19-3 \quad R = \frac{1}{fC}$$

$$19-4 \quad A_v = -\frac{C_1}{C_2}$$

SELF-TEST

Answers are at the end of the chapter.

- The acronym FPAA stands for
 - field-programmable amplifier array
 - fast-programmable analog array
 - field-programmable analog array
 - feedback path analog amplifier
- FPAAs contain CABs, which are
 - configuration analog blocks
 - capacitor actuated blocks
 - configurable amplifier blocks
 - constant amplification blocks
- During reprogramming of an FPAA running in a system, the first memory into which reconfiguration data are stored is the
 - configuration RAM
 - look-up table
 - main memory
 - shadow RAM
- A circuit technology commonly used to implement designs in FPAAs is
 - switched-inductor circuits
 - emulated resistor networks
 - switched-capacitor circuits
 - AMI
- A typical setup for programming an FPAA must include
 - a computer, an FPAA chip on a development board, development software, a standard interface, and a bezel tester
 - a computer, an FPAA chip on a development board, development software, and a signal generator
 - a computer, an FPAA chip on a development board, development software, and a standard interface to connect the computer and development board
- The dynamic reconfiguration of an FPAA is the same as
 - on-the-fly reprogramming
 - static configuration
 - downloading
 - simulation
- A CAM is
 - a constant analog multiplier
 - a configurable analog module
 - a configurable analog matrix
 - a capacitor adjustable module
- For best results, you should implement the software design of an analog circuit in an FPAA by
 - selecting appropriate CAMs, interconnecting them to each other and to inputs and outputs, and downloading to the FPAA
 - selecting appropriate CAMs, interconnecting them to each other and to inputs and outputs, running a simulation, and downloading to the FPAA if the simulation is successful
 - selecting appropriate CABs, interconnecting them to each other and to inputs and outputs, running a simulation, downloading to the FPAA if the simulation is successful, and testing the FPAA

PROBLEMS

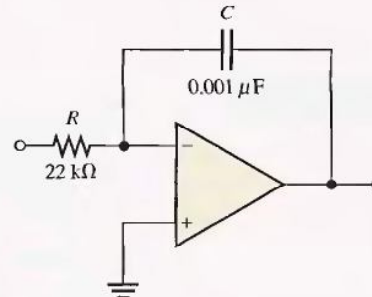
Answers to all odd-numbered problems are at the end of the book.

SECTION 19-2 Switched-Capacitor Circuits

- The capacitor in a switched-capacitor circuit has a value of 2200 pF and is switched with a waveform having a period of 10 μ s. Determine the value of the resistor that it emulates.
- In a switched-capacitor circuit, the 100 pF capacitor is switched at a frequency of 8 kHz. What resistor value is emulated?

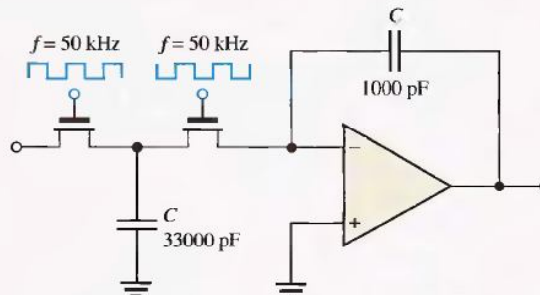
- Replace the integrator in Figure 19–29 with one that uses a switched-capacitor with a capacitance value of 2200 pF to emulate the resistor. Show the circuit and specify the frequency at which the capacitor must be switched.

► **FIGURE 19–29**



- Replace the integrator in Figure 19–29 with one that uses a switched-capacitor with a capacitance value of 330 pF to emulate the resistor. Show the circuit and specify the frequency at which the capacitor must be switched.
- Determine the resistance that is emulated in the integrator in Figure 19–30.

► **FIGURE 19–30**



- Implement a differentiator using a switched-capacitor circuit with a fixed input capacitor of 0.01 μF. Use a switching frequency of 200 kHz to achieve an effective resistance of 15 kΩ.

SECTION 19–4 FPAA Programming

The following problems require the AnadigmDesigner2 software that can be downloaded for a free 60-day trial period. The website address is www.anadigm.com.

- Using the software, implement an inverting amplifier with a gain of 20. Simulate the circuit using a 20 kHz input sine wave with a peak amplitude of 100 mV. Verify that the circuit is operating as expected.
- Using the software, implement a noninverting amplifier with a gain of 30. Simulate the circuit using a 100 kHz input sine wave with a peak amplitude of 10 mV. Verify that the circuit is operating as expected.
- Using the software, implement a noninverting low-pass filter with a cutoff (corner) frequency of 10 kHz and a gain of 1. Using simulation, verify that the circuit is operating as expected. Choose an appropriate input voltage amplitude.
- Using the software, implement a two-stage noninverting amplifier with an overall gain of 100. Simulate the circuit using a 100 kHz input sine wave with an amplitude of 20 mV. Verify that the circuit is operating as expected.
- Using the software, implement an integrator with an output rate of change or integration constant of 2 V/μs. Simulate the circuit using an appropriate square wave input to verify that it is operating as expected.
- Using the software, implement a differentiator with a constant of 0.1 μs. Simulate the circuit using an appropriate triangular wave input. Verify that the circuit is operating as expected.
- Using the software, implement an inverting band-pass filter with a center frequency of 15 kHz, a gain of 1, and a Q of 10. Using simulation, verify that the circuit is operating as expected.

14. Using the software, implement an inverting high-pass filter with a cutoff (corner) frequency of 20 kHz and a gain of 1. Using simulation, verify that the circuit is operating as expected. Apply an input signal of 1 V.

ANSWERS

SECTION REVIEWS

SECTION 19-1 The Field-Programmable Analog Array (FPAA)

1. FPAA is field-programmable analog array.
2. CAB is configurable analog block.
3. CABs and the interconnection network are FPAA programmable features.
4. Switched-capacitor networks

SECTION 19-2 Switched-Capacitor Circuits

1. Switched-capacitor circuits are used to emulate resistors.
2. By moving the same amount of charge corresponding to the current in the equivalent resistance
3. The resistance is determined by the switching frequency and the capacitance value.
4. MOSFETs are used for switches.

SECTION 19-3 A Specific FPAA

1. An AN221E04 FPAA CAB contains two op-amps, a comparator, control logic, RAMs, clock generator, LUT interface, SAR logic, and output interface.
2. The shadow RAM and the configuration RAM
3. The switch matrix provides for programmable interconnections and implementation of switched-capacitor circuits within a CAB.
4. The NOL clock generator provides non-overlapping clock signals for the switched-capacitor operation.

SECTION 19-4 FPAA Programming

1. Development software provides for entering a circuit design on the computer, simulating the design, and downloading the design to the FPAA chip.
2. A CAM is a configurable analog module.
3. Downloading implements the software circuit in hardware (FPAA).
4. Static reconfiguration is the process of changing the design in a FPAA, requiring power down or reset. Dynamic reconfiguration allows a new design or design modification to be made while the FPAA is operating in a system without reset.
5. The term “*on-the-fly*”, used to describe FPAA reconfiguration, means the same thing as dynamic reconfiguration.

RELATED PROBLEM FOR EXAMPLE

19-1 178.57 kHz

SELF-TEST

1. (b) 2. (a) 3. (d) 4. (c) 5. (c) 6. (a) 7. (b) 8. (c)

A: Table of Standard Resistor Values

Resistance Tolerance ($\pm\%$)

0.1%				0.1%				0.1%				0.1%				0.1%				0.1%			
0.25%	1%	2%	10%	0.25%	1%	2%	10%	0.25%	1%	2%	10%	0.25%	1%	2%	10%	0.25%	1%	2%	10%	0.25%	1%	2%	10%
0.5%		5%		0.5%		5%		0.5%		5%		0.5%		5%		0.5%		5%		0.5%		5%	
10.0	10.0	10	10	14.7	14.7	—	—	21.5	21.5	—	—	31.6	31.6	—	—	46.4	46.4	—	—	68.1	68.1	68	68
10.1	—	—	—	14.9	—	—	—	21.8	—	—	—	32.0	—	—	—	47.0	—	47	47	69.0	—	—	—
10.2	10.2	—	—	15.0	15.0	15	15	22.1	22.1	22	22	32.4	32.4	—	—	47.5	47.5	—	—	69.8	69.8	—	—
10.4	—	—	—	15.2	—	—	—	22.3	—	—	—	32.8	—	—	—	48.1	—	—	—	70.6	—	—	—
10.5	10.5	—	—	15.4	15.4	—	—	22.6	22.6	—	—	33.2	33.2	33	33	48.7	48.7	—	—	71.5	71.5	—	—
10.6	—	—	—	15.6	—	—	—	22.9	—	—	—	33.6	—	—	—	49.3	—	—	—	72.3	—	—	—
10.7	10.7	—	—	15.8	15.8	—	—	23.2	23.2	—	—	34.0	34.0	—	—	49.9	49.9	—	—	73.2	73.2	—	—
10.9	—	—	—	16.0	—	16	—	23.4	—	—	—	34.4	—	—	—	50.5	—	—	—	74.1	—	—	—
11.0	11.0	11	—	16.2	16.2	—	—	23.7	23.7	—	—	34.8	34.8	—	—	51.1	51.1	51	—	75.0	75.0	75	—
11.1	—	—	—	16.4	—	—	—	24.0	—	24	—	35.2	—	—	—	51.7	—	—	—	75.9	—	—	—
11.3	11.3	—	—	16.5	16.5	—	—	24.3	24.3	—	—	35.7	35.7	—	—	52.3	52.3	—	—	76.8	76.8	—	—
11.4	—	—	—	16.7	—	—	—	24.6	—	—	—	36.1	—	36	—	53.0	—	—	—	77.7	—	—	—
11.5	11.5	—	—	16.9	16.9	—	—	24.9	24.9	—	—	36.5	36.5	—	—	53.6	53.6	—	—	78.7	78.7	—	—
11.7	—	—	—	17.2	—	—	—	25.2	—	—	—	37.0	—	—	—	54.2	—	—	—	79.6	—	—	—
11.8	11.8	—	—	17.4	17.4	—	—	25.5	25.5	—	—	37.4	37.4	—	—	54.9	54.9	—	—	80.6	80.6	—	—
12.0	—	12	12	17.6	—	—	—	25.8	—	—	—	37.9	—	—	—	56.2	—	—	—	81.6	—	—	—
12.1	12.1	—	—	17.8	17.8	—	—	26.1	26.1	—	—	38.3	38.3	—	—	56.6	56.6	56	56	82.5	82.5	82	82
12.3	—	—	—	18.0	—	18	18	26.4	—	—	—	38.8	—	—	—	56.9	—	—	—	83.5	—	—	—
12.4	12.4	—	—	18.2	18.2	—	—	26.7	26.7	—	—	39.2	39.2	39	39	57.6	57.6	—	—	84.5	84.5	—	—
12.6	—	—	—	18.4	—	—	—	27.1	—	27	27	39.7	—	—	—	58.3	—	—	—	85.6	—	—	—
12.7	12.7	—	—	18.7	18.7	—	—	27.4	27.4	—	—	40.2	40.2	—	—	59.0	59.0	—	—	86.6	86.6	—	—
12.9	—	—	—	18.9	—	—	—	27.7	—	—	—	40.7	—	—	—	59.7	—	—	—	87.6	—	—	—
13.0	13.0	13	—	19.1	19.1	—	—	28.0	28.0	—	—	41.2	41.2	—	—	60.4	60.4	—	—	88.7	88.7	—	—
13.2	—	—	—	19.3	—	—	—	28.4	—	—	—	41.7	—	—	—	61.2	—	—	—	89.8	—	—	—
13.3	13.3	—	—	19.6	19.6	—	—	28.7	28.7	—	—	42.2	42.2	—	—	61.9	61.9	62	—	90.9	90.9	91	—
13.5	—	—	—	19.8	—	—	—	29.1	—	—	—	42.7	—	—	—	62.6	—	—	—	92.0	—	—	—
13.7	13.7	—	—	20.0	20.0	20	—	29.4	29.4	—	—	43.2	43.2	43	—	63.4	63.4	—	—	93.1	93.1	—	—
13.8	—	—	—	20.3	—	—	—	29.8	—	—	—	43.7	—	—	—	64.2	—	—	—	94.2	—	—	—
14.0	14.0	—	—	20.5	20.5	—	—	30.1	30.1	30	—	44.2	44.2	—	—	64.9	64.9	—	—	95.3	95.3	—	—
14.2	—	—	—	20.8	—	—	—	30.5	—	—	—	44.8	—	—	—	65.7	—	—	—	96.5	—	—	—
14.3	14.3	—	—	21.0	21.0	—	—	30.9	30.9	—	—	45.3	45.3	—	—	66.5	66.5	—	—	97.6	97.6	—	—
14.5	—	—	—	21.3	—	—	—	31.2	—	—	—	45.9	—	—	—	67.3	—	—	—	98.8	—	—	—

NOTE: These values are generally available in multiples of 0.1, 1, 10, 100, 1 k, and 1 M.

B: Derivations of Selected Equations

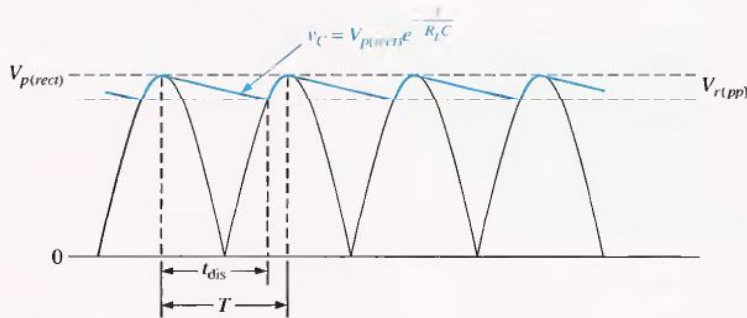
EQUATION 2-1

The average value of a half-wave rectified sine wave is the area under the curve divided by the period (2π). The equation for a sine wave is

$$\begin{aligned}
 v &= V_p \sin \theta \\
 V_{\text{AVG}} &= \frac{\text{area}}{2\pi} = \frac{1}{2\pi} \int_0^\pi V_p \sin \theta \, d\theta = \frac{V_p}{2\pi} (-\cos \theta) \Big|_0^\pi \\
 &= \frac{V_p}{2\pi} [-\cos \pi - (-\cos 0)] = \frac{V_p}{2\pi} [-(-1) - (-1)] = \frac{V_p}{2\pi} (2) \\
 V_{\text{AVG}} &= \frac{V_p}{\pi}
 \end{aligned}$$

EQUATION 2-11

Refer to Figure B-1.



▲ FIGURE B-1

When the filter capacitor discharges through R_L , the voltage is

$$v_C = V_{p(\text{rect})} e^{-t/R_L C}$$

Since the discharge time of the capacitor is from one peak to approximately the next peak, $t_{\text{dis}} \cong T$ when v_C reaches its minimum value.

$$v_{C(\text{min})} = V_{p(\text{rect})} e^{-T/R_L C}$$

Since $RC \gg T$, $T/R_L C$ becomes much less than 1 (which is usually the case); $e^{-T/R_L C}$ approaches 1 and can be expressed as

$$e^{-T/R_L C} \cong 1 - \frac{T}{R_L C}$$

Therefore,

$$v_{C(\text{min})} = V_{p(\text{rect})} \left(1 - \frac{T}{R_L C} \right)$$

The peak-to-peak ripple voltage is

$$V_{r(pp)} = V_{p(rect)} - V_{C(min)} = V_{p(rect)} - V_{p(rect)} + \frac{V_{p(rect)}T}{R_L C} = \frac{V_{p(rect)}T}{R_L C}$$

$$V_{r(pp)} \cong \left(\frac{1}{fR_L C} \right) V_{p(rect)}$$

EQUATION 2-12

To obtain the dc value, one-half of the peak-to-peak ripple is subtracted from the peak value.

$$V_{DC} = V_{p(rect)} - \frac{V_{r(pp)}}{2} = V_{p(rect)} - \left(\frac{1}{2fR_L C} \right) V_{p(rect)}$$

$$V_{DC} = \left(1 - \frac{1}{2fR_L C} \right) V_{p(rect)}$$

EQUATION 6-1

The Shockley equation for the base-emitter pn junction is

$$I_E = I_R(e^{VQ/kT} - 1)$$

where I_E = the total forward current across the base-emitter junction

I_R = the reverse saturation current

V = the voltage across the depletion layer

Q = the charge on an electron

k = a number known as Boltzmann's constant

T = the absolute temperature

At ambient temperature, $Q/kT \cong 40$, so

$$I_E = I_R(e^{V40} - 1)$$

Differentiating yields

$$\frac{dI_E}{dV} = 40I_R e^{V40}$$

Since $I_R e^{V40} = I_E + I_R$,

$$\frac{dI_E}{dV} = 40(I_E + I_R)$$

Assuming $I_R \ll I_E$,

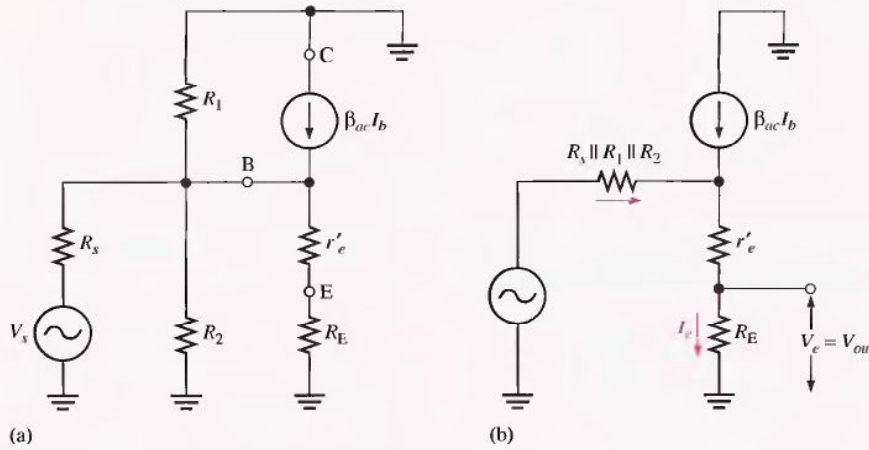
$$\frac{dI_E}{dV} \cong 40I_E$$

The ac resistance r'_e of the base-emitter junction can be expressed as dV/dI_E .

$$r'_e = \frac{dV}{dI_E} \cong \frac{1}{40I_E} \cong \frac{25 \text{ mV}}{I_E}$$

EQUATION 6-14

The emitter-follower is represented by the r parameter ac equivalent circuit in Figure B-2(a).



▲ **FIGURE B-2**

By thevenizing from the base back to the source, the circuit is simplified to the form shown in Figure B-2(b).

$$V_{out} = V_e, I_{out} = I_e, \text{ and } I_{in} = I_b$$

$$R_{out} = \frac{V_e}{I_e}$$

$$I_e \cong \beta_{ac} I_b$$

With $V_s = 0$ and with I_b produced by V_{out} , and neglecting the base-to-emitter voltage drop (and therefore r'_e),

$$I_b \cong \frac{V_e}{R_1 \parallel R_2 \parallel R_s}$$

Assuming that $R_1 \gg R_s$ and $R_2 \gg R_s$,

$$I_b \cong \frac{V_e}{R_s}$$

$$I_{out} = I_e = \frac{\beta_{ac} V_e}{R_s}$$

$$\frac{V_{out}}{I_{out}} = \frac{V_e}{I_e} = \frac{V_e}{\beta_{ac} V_e / R_s} = \frac{R_s}{\beta_{ac}}$$

Looking into the emitter, R_E appears in parallel with R_s/β_{ac} . Therefore,

$$R_{out} = \left(\frac{R_s}{\beta_{ac}} \right) \parallel R_E$$

MIDPOINT BIAS (CHAPTER 7)

The following proof is for the equation on page 345 that shows $I_D \cong 0.5 I_{DSS}$ when $V_{GS} = V_{GS(off)}/3.4$.

Start with Equation 7-1:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

Let $I_D = 0.5I_{DSS}$.

$$0.5I_{DSS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

Cancelling I_{DSS} on each side,

$$0.5 = \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

We want a factor (call it F) by which $V_{GS(off)}$ can be divided to give a value of V_{GS} that will produce a drain current that is $0.5I_{DSS}$.

$$0.5 = \left[1 - \frac{\left(\frac{V_{GS(off)}}{F} \right)}{V_{GS(off)}} \right]^2$$

Solving for F ,

$$\begin{aligned} \sqrt{0.5} &= 1 - \frac{\left(\frac{V_{GS(off)}}{F} \right)}{V_{GS(off)}} = 1 - \frac{1}{F} \\ \sqrt{0.5} - 1 &= -\frac{1}{F} \\ \frac{1}{F} &= 1 - \sqrt{0.5} \\ F &= \frac{1}{1 - \sqrt{0.5}} \cong 3.4 \end{aligned}$$

Therefore, $I_D \cong 0.5I_{DSS}$ when $V_{GS} = V_{GS(off)}/3.4$.

EQUATION 8-5

$$\begin{aligned} I_D &= I_{DSS} \left(1 - \frac{I_D R_S}{V_{GS(off)}} \right)^2 = I_{DSS} \left(1 - \frac{I_D R_S}{V_{GS(off)}} \right) \left(1 - \frac{I_D R_S}{V_{GS(off)}} \right) \\ &= I_{DSS} \left(1 - \frac{2I_D R_S}{V_{GS(off)}} + \frac{I_D^2 R_S^2}{V_{GS(off)}^2} \right) = I_{DSS} - \frac{2I_{DSS} R_S}{V_{GS(off)}} I_D + \frac{I_{DSS} R_S^2}{V_{GS(off)}^2} I_D^2 \end{aligned}$$

Rearranging into a standard quadratic equation form,

$$\left(\frac{I_{DSS} R_S^2}{V_{GS(off)}^2} \right) I_D^2 - \left(1 + \frac{2I_{DSS} R_S}{V_{GS(off)}} \right) I_D + I_{DSS} = 0$$

The coefficients and constant are

$$\begin{aligned} A &= \frac{R_S^2 I_{DSS}}{V_{GS(off)}^2} \\ B &= - \left(1 + \frac{2R_S I_{DSS}}{V_{GS(off)}} \right) \\ C &= I_{DSS} \end{aligned}$$

In simplified notation, the equation is

$$AI_D^2 + BI_D + C = 0$$

The solutions to this quadratic equation are

$$I_D = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

EQUATION 10-1

An inverting amplifier with feedback capacitance is shown in Figure B-3. For the input,

$$I_1 = \frac{V_1 - V_2}{X_C}$$

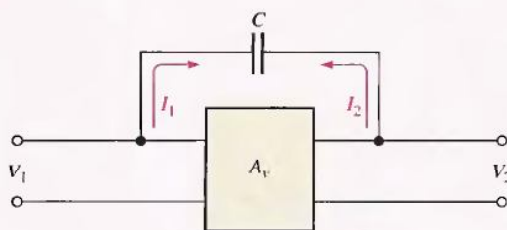
Factoring V_1 out,

$$I_1 = \frac{V_1(1 - V_2/V_1)}{X_C}$$

The ratio V_2/V_1 is the voltage gain, $-A_v$.

$$I_1 = \frac{V_1(1 + A_v)}{X_C} = \frac{V_1}{X_C/(1 + A_v)}$$

► FIGURE B-3



The effective reactance as seen from the input terminals is

$$X_{C_{in(Miller)}} = \frac{X_C}{1 + A_v}$$

or

$$\frac{1}{2\pi f C_{in(Miller)}} = \frac{1}{2\pi f C(1 + A_v)}$$

Cancelling and inverting,

$$C_{in(Miller)} = C(A_v + 1)$$

EQUATION 10-2

For the output in Figure B-3,

$$I_2 = \frac{V_2 - V_1}{X_C} = \frac{V_2(1 - V_1/V_2)}{X_C}$$

Since $V_1/V_2 = -1/A_v$,

$$I_2 = \frac{V_2(1 + 1/A_v)}{X_C} = \frac{V_2}{X_C/(1 + 1/A_v)} = \frac{V_2}{X_C/[(A_v + 1)/A_v]}$$

The effective reactance as seen from the output is

$$X_{C_{out(Miller)}} = \frac{X_C}{(A_v + 1)/A_v}$$

$$\frac{1}{2\pi f C_{out(Miller)}} = \frac{1}{2\pi f C [(A_v + 1)/A_v]}$$

Cancelling and inverting yields

$$C_{out(Miller)} = C \left(\frac{A_v + 1}{A_v} \right)$$

EQUATIONS 10-29 AND 10-30

The total gain, $A_{v(tot)}$, of an individual amplifier stage at the lower critical frequency equals the midrange gain, $A_{v(mid)}$, times the attenuation of the high-pass RC circuit.

$$A_{v(tot)} = A_{v(mid)} \left(\frac{R}{\sqrt{R^2 + X_C^2}} \right) = A_{v(mid)} \left(\frac{1}{\sqrt{1 + X_C^2/R^2}} \right)$$

$$f_{cl} = \frac{1}{2\pi RC}$$

Dividing both sides by any frequency f ,

$$\frac{f_{cl}}{f} = \frac{1}{(2\pi f C)R}$$

Since $X_C = 1/2\pi f C$,

$$\frac{f_{cl}}{f} = \frac{X_C}{R}$$

Substitution in the gain formula gives

$$A_{v(tot)} = A_{v(mid)} \left(\frac{1}{\sqrt{1 + (f_{cl}/f)^2}} \right)$$

The gain ratio is

$$\frac{A_{v(tot)}}{A_{v(mid)}} = \frac{1}{\sqrt{1 + (f_{cl}/f)^2}}$$

For a multistage amplifier with n stages, each with the same f_{cl} and gain ratio, the product of the gain ratios is

$$\left(\frac{1}{\sqrt{1 + (f_{cl}/f)^2}} \right)^n$$

The critical frequency f'_{cl} of the multistage amplifier is the frequency at which $A_{v(tot)} = 0.707A_{v(mid)}$, so the gain ratio at f'_{cl} is

$$\frac{A_{v(tot)}}{A_{v(mid)}} = 0.707 = \frac{1}{1.414} = \frac{1}{\sqrt{2}}$$

Therefore, for a multistage amplifier,

$$\frac{1}{\sqrt{2}} = \left[\frac{1}{\sqrt{1 + (f_{cl}/f'_{cl})^2}} \right]^n = \frac{1}{(\sqrt{1 + (f_{cl}/f'_{cl})^2})^n}$$

So

$$2^{1/2} = (\sqrt{1 + (f_{cl}/f'_{cl})^2})^n$$

Squaring both sides,

$$2 = (1 + (f_{cl}/f'_{cl})^2)^n$$

Taking the n th root of both sides,

$$2^{1/n} = 1 + (f_{cl}/f'_{cl})^2$$

$$\left(\frac{f_{cl}}{f'_{cl}}\right)^2 = 2^{1/n} - 1$$

$$\left(\frac{f_{cl}}{f'_{cl}}\right) = \sqrt{2^{1/n} - 1}$$

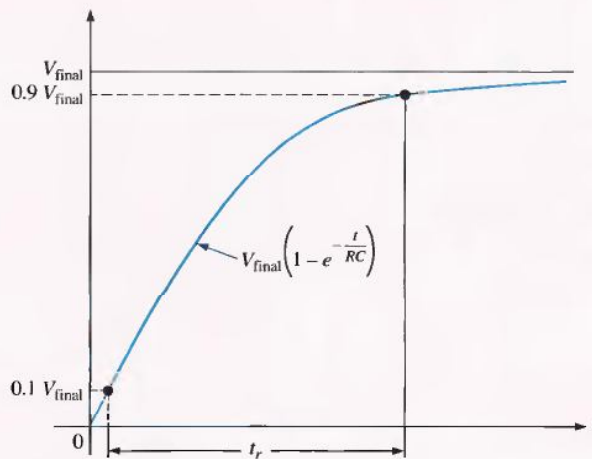
$$f'_{cl} = \frac{f_{cl}}{\sqrt{2^{1/n} - 1}}$$

A similar process will give Equation 10-30:

$$f'_{cu} = f_{cu} \sqrt{2^{1/n} - 1}$$

EQUATIONS 10-31 AND 10-32

The *rise time* is defined as the time required for the voltage to increase from 10 percent of its final value to 90 percent of its final value, as indicated in Figure B-4.



▲ FIGURE B-4

Expressing the curve in its exponential form gives

$$v = V_{\text{final}}(1 - e^{-t/RC})$$

When $v = 0.1V_{\text{final}}$,

$$0.1V_{\text{final}} = V_{\text{final}}(1 - e^{-t/RC}) = V_{\text{final}} - V_{\text{final}}e^{-t/RC}$$

$$V_{\text{final}}e^{-t/RC} = 0.9V_{\text{final}}$$

$$e^{-t/RC} = 0.9$$

$$\ln e^{-t/RC} = \ln(0.9)$$

$$-\frac{t}{RC} = -0.1$$

$$t = 0.1RC$$

When $v = 0.9V_{\text{final}}$,

$$\begin{aligned} 0.9V_{\text{final}} &= V_{\text{final}}(1 - e^{-t/RC}) = V_{\text{final}} - V_{\text{final}}e^{-t/RC} \\ V_{\text{final}}e^{-t/RC} &= 0.1V_{\text{final}} \\ \ln e^{-t/RC} &= \ln(0.1) \\ -\frac{t}{RC} &= -2.3 \\ t &= 2.3RC \end{aligned}$$

The difference is the rise time.

$$t_r = 2.3RC - 0.1RC = 2.2RC$$

The critical frequency of an RC circuit is

$$\begin{aligned} f_c &= \frac{1}{2\pi RC} \\ RC &= \frac{1}{2\pi f_c} \end{aligned}$$

Substituting,

$$\begin{aligned} t_r &= \frac{2.2}{2\pi f_{cu}} = \frac{0.35}{f_{cu}} \\ f_{cu} &= \frac{0.35}{t_r} \end{aligned}$$

In a similar way, it can be shown that

$$f_{cl} = \frac{0.35}{t_f}$$

EQUATION 12-21

The formula for open-loop gain in Equation 12-19 can be expressed in complex notation as

$$A_{ol} = \frac{A_{ol(mid)}}{1 + jf/f_{c(ol)}}$$

Substituting the above expression into the equation $A_{cl} = A_{ol}/(1 + BA_{ol})$ gives a formula for the total closed-loop gain.

$$A_{cl} = \frac{A_{ol(mid)}/(1 + jf/f_{c(ol)})}{1 + BA_{ol(mid)}/(1 + jf/f_{c(ol)})}$$

Multiplying the numerator and denominator by $1 + jf/f_{c(ol)}$ yields

$$A_{cl} = \frac{A_{ol(mid)}}{1 + BA_{ol(mid)} + jf/f_{c(ol)}}$$

Dividing the numerator and denominator by $1 + BA_{ol(mid)}$ gives

$$A_{cl} = \frac{A_{ol(mid)} / (1 + BA_{ol(mid)})}{1 + j[f / (f_{c(ol)}(1 + BA_{ol(mid)}))]}$$

The above expression is of the form of the first equation

$$A_{cl} = \frac{A_{cl(mid)}}{1 + jf/f_{c(cl)}}$$

where $f_{c(cl)}$ is the closed-loop critical frequency. Thus,

$$f_{c(cl)} = f_{c(ol)}(1 + BA_{ol(mid)})$$

EQUATION 16-1

$$\frac{V_{out}}{V_{in}} = \frac{R(-jX)/(R - jX)}{(R - jX) + R(-jX)/(R - jX)} = \frac{R(-jX)}{(R - jX)^2 - jRX}$$

Multiplying the numerator and denominator by j ,

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{RX}{j(R - jX)^2 + RX} = \frac{RX}{RX + j(R^2 - j2RX - X^2)} \\ &= \frac{RX}{RX + jR^2 + 2RX - jX^2} = \frac{RX}{3RX + j(R^2 - X^2)} \end{aligned}$$

For a 0° phase angle there can be no j term. Recall from complex numbers in ac theory that a *nonzero* angle is associated with a complex number having a j term. Therefore, at f_r the j term is 0.

$$R^2 - X^2 = 0$$

Thus,

$$\frac{V_{out}}{V_{in}} = \frac{RX}{3RX}$$

Cancelling yields

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

EQUATION 16-2

From the derivation of Equation 16-1,

$$\begin{aligned} R^2 - X^2 &= 0 \\ R^2 &= X^2 \\ R &= X \end{aligned}$$

Since $X = \frac{1}{2\pi f_r C}$,

$$\begin{aligned} R &= \frac{1}{2\pi f_r C} \\ f_r &= \frac{1}{2\pi RC} \end{aligned}$$

EQUATIONS 16-3 AND 16-4

The feedback circuit in the phase-shift oscillator consists of three RC stages, as shown in Figure B-5. An expression for the attenuation is derived using the mesh analysis method for the loop assignment shown. All R s are equal in value, and all C s are equal in value.

$$\begin{aligned}(R - j1/2\pi fC)I_1 - RI_2 + 0I_3 &= V_{in} \\ -RI_1 + (2R - j1/2\pi fC)I_2 - RI_3 &= 0 \\ 0I_1 - RI_2 + (2R - j1/2\pi fC)I_3 &= 0\end{aligned}$$

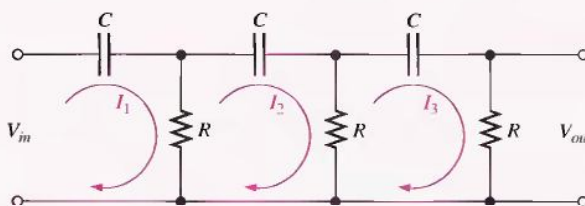


FIGURE B-5

In order to get V_{out} , we must solve for I_3 using determinants:

$$\begin{aligned}I_3 &= \frac{\begin{vmatrix} (R - j1/2\pi fC) & -R & V_{in} \\ -R & (2R - j1/2\pi fC) & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} (R - j1/2\pi fC) & -R & 0 \\ -R & (2R - j1/2\pi fC) & -R \\ 0 & -R & (2R - j1/2\pi fC) \end{vmatrix}} \\ I_3 &= \frac{R^2 V_{in}}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^2(2R - j1/2\pi fC) - R^2(R - j1/2\pi fC)} \\ \frac{V_{out}}{V_{in}} &= \frac{RI_3}{V_{in}} \\ &= \frac{R^3}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^2(2R - j1/2\pi fC) - R^2(R - j1/2\pi fC)} \\ &= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3[(2 - j1/2\pi fRC) - (1 - j1/2\pi fRC)]} \\ &= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3(3 - j1/2\pi fRC)} \\ \frac{V_{out}}{V_{in}} &= \frac{1}{(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - (3 - j1/2\pi fRC)}\end{aligned}$$

Expanding and combining the real terms and the j terms separately.

$$\frac{V_{out}}{V_{in}} = \frac{1}{\left(1 - \frac{5}{4\pi^2 f^2 R^2 C^2}\right) - j\left(\frac{6}{2\pi fRC} - \frac{1}{(2\pi f)^3 R^3 C^3}\right)}$$

For oscillation in the phase-shift amplifier, the phase shift through the RC circuit must equal 180° . For this condition to exist, the j term must be 0 at the frequency of oscillation f_r .

$$\begin{aligned}\frac{6}{2\pi f_r RC} - \frac{1}{(2\pi f_r)^3 R^3 C^3} &= 0 \\ \frac{6(2\pi)^2 f_r^2 R^2 C^2 - 1}{(2\pi)^3 f_r^3 R^3 C^3} &= 0 \\ 6(2\pi)^2 f_r^2 R^2 C^2 - 1 &= 0 \\ f_r^2 &= \frac{1}{6(2\pi)^2 R^2 C^2} \\ f_r &= \frac{1}{2\pi\sqrt{6RC}}\end{aligned}$$

Since the j term is 0,

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - \frac{5}{4\pi^2 f_r^2 R^2 C^2}} = \frac{1}{1 - \frac{5}{\left(\frac{1}{\sqrt{6RC}}\right)^2 R^2 C^2}} = \frac{1}{1 - 30} = -\frac{1}{29}$$

The negative sign results from the 180° inversion. Thus, the value of attenuation for the feedback circuit is

$$B = \frac{1}{29}$$

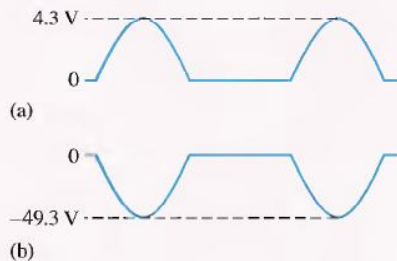
Answers To Odd-Numbered Problems

Chapter 1

1. 6 electrons; 6 protons
3. (a) insulator (b) semiconductor (c) conductor
5. Four
7. Conduction band and valence band
9. Antimony is a pentavalent material. Boron is a trivalent material. Both are used for doping.
11. No. The barrier potential is a voltage drop.
13. To prevent excessive forward current.
15. A temperature increase.
17. (a) -3 V (b) 0.7 V (c) 0.7 V (d) 0.7 V
19. $V_A = 25\text{ V}$; $V_B = 24.3\text{ V}$; $V_C = 8.7\text{ V}$; $V_D = 8\text{ V}$
21. Diode open
23. Diode shorted
25. Diode shorted
27. Diode open

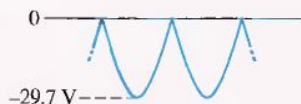
Chapter 2

1. See Figure ANS-1.



▲ FIGURE ANS-1

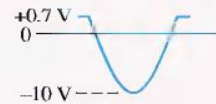
3. 23 V rms
5. (a) 1.59 V (b) 63.7 V (c) 16.4 V (d) 10.5 V
7. 173 V
9. 78.5 V
11. See Figure ANS-2.



▲ FIGURE ANS-2

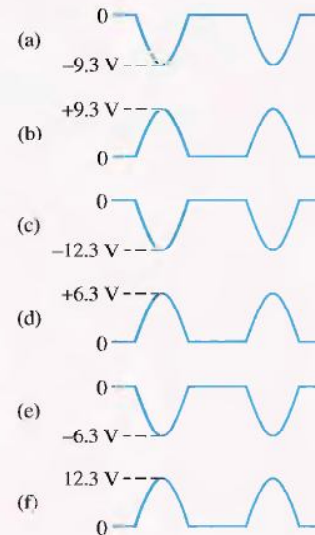
13. $V_r = 8.33\text{ V}$; $V_{DC} = 25.8\text{ V}$
15. $556\text{ }\mu\text{F}$

17. $V_{r(pp)} = 1.25\text{ V}$; $V_{DC} = 48.9\text{ V}$
19. 4%
21. See Figure ANS-3.



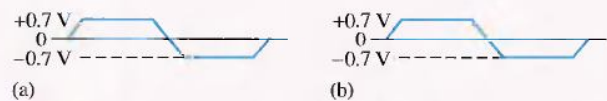
▲ FIGURE ANS-3

23. See Figure ANS-4.



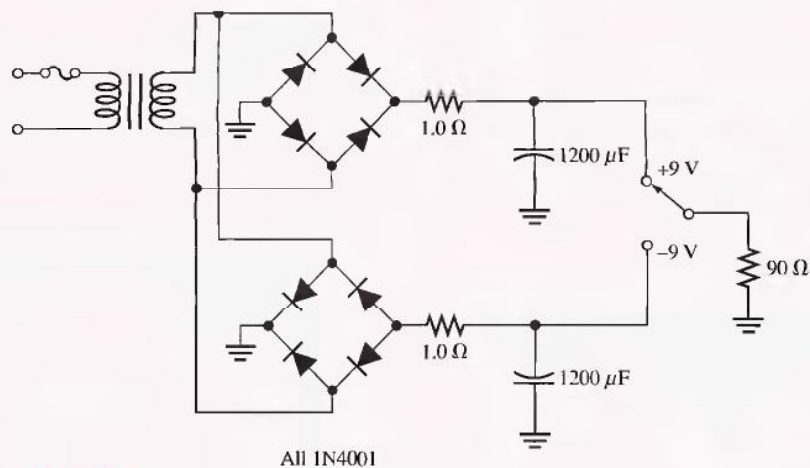
▲ FIGURE ANS-4

25. See Figure ANS-5.



▲ FIGURE ANS-5

27. (a) A sine wave with a positive peak at $+0.7\text{ V}$, a negative peak at -7.3 V , and a dc value of -3.3 V .
- (b) A sine wave with a positive peak at $+29.3\text{ V}$, a negative peak at -0.7 V , and a dc value of $+14.3\text{ V}$.
- (c) A square wave varying from $+0.7\text{ V}$ down to -15.3 V , with a dc value of -7.3 V .
- (d) A square wave varying from $+1.3\text{ V}$ down to -0.7 V , with a dc value of $+0.3\text{ V}$.
29. 56.6 V

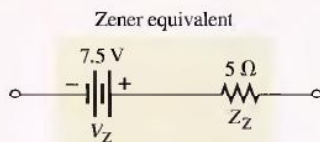


▲ FIGURE ANS-6

31. 50 V
33. 62.5 mΩ
35. R_{surge} is open. Capacitor is shorted.
37. The circuit should not fail because the diode ratings exceed the actual PIV and maximum current.
39. Excessive PIV or surge current causes diode to open each time power is turned on. It could be a faulty transformer or maybe the diodes do not have sufficient PIV rating.
41. 177 μF
43. 651 mΩ (nearest standard 0.68 Ω)
45. See Figure ANS-6.
47. $V_{C1} = 155 \text{ V}$; $V_{C2} = 310 \text{ V}$
49. Diode leaky
51. Bottom diode open
53. Open filter capacitor
55. D_1 open

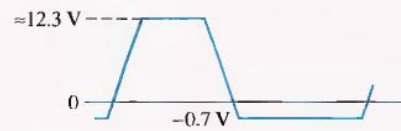
Chapter 3

1. See Figure ANS-7.



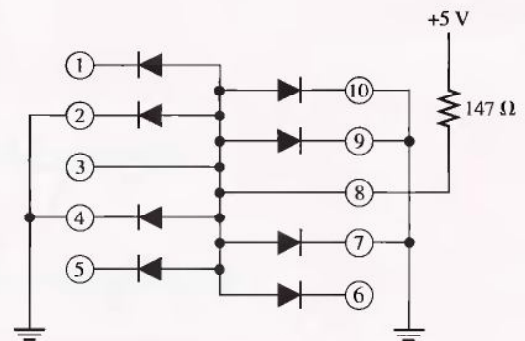
▲ FIGURE ANS-7

3. 5 Ω
5. 6.92 V
7. 14.3 V
9. See Figure ANS-8.



▲ FIGURE ANS-8

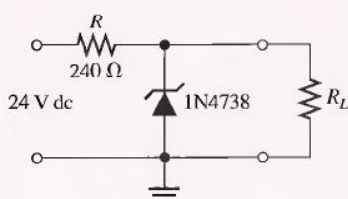
11. 14.3%
13. 3.13%
15. 5.88%
17. 3 V
19. $\approx 2.5 \text{ V}$
21. See Figure ANS-9.



▲ FIGURE ANS-9

23. (a) 30 k Ω (b) 8.57 k Ω (c) 5.88 k Ω
25. -750 Ω
27. The reflective ends cause the light to bounce back and forth, thus increasing the intensity of the light. The partially reflective end allows a portion of the reflected light to be emitted.

29. (a) ≈ 30 V dc
 (b) 0 V
 (c) Excessive 120 Hz ripple limited to 12 V by zener
 (d) Full-wave rectified waveform limited at 12 V by zener
 (e) 60 Hz ripple limited to 12 V
 (f) 60 Hz ripple limited to 12 V
 (g) 0 V
 (h) 0 V
31. Could be fuse, transformer, limiting resistor, or surge resistor open. Also, capacitor or zener could be shorted. Cannot isolate further with given measurements.
33. D_1 open, R_1 open, no dc voltage, short in threshold circuit
35. (a) 60 V (b) 307 mW
 (c) 1.27 W (d) 21 pF
 (e) 1N5139 (f) 4.82 pF
37. (a) Reverse-bias voltage (b) 940 nm
 (c) 40 nA (d) 940 nm
 (e) $40 \mu\text{A}/\text{mW}/\text{cm}^2$ (f) $104 \mu\text{A}$
39. $V_{\text{OUT}(1)} = 6.8$ V; $V_{\text{OUT}(2)} = 24$ V
41. See Figure ANS-10.

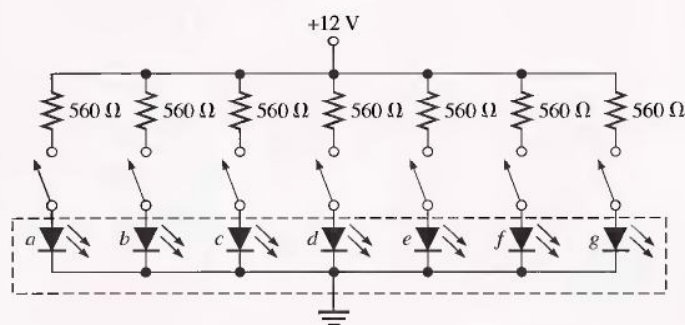


▲ FIGURE ANS-10

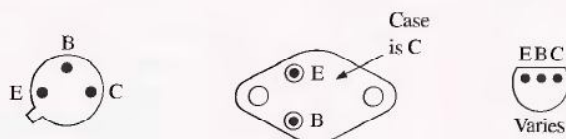
43. See Figure ANS-11.
 45. Zener diode open
 47. Zener diode shorted

Chapter 4

- Holes
- The base is narrow and lightly doped so that a small recombination (base) current is generated compared to the collector current.
- Negative, positive
- 0.947
- 101.5
- 8.98 mA
- 0.99
- (a) $V_{\text{BE}} = 0.7$ V, $V_{\text{CE}} = 5.10$ V, $V_{\text{CB}} = +4.40$ V
 (b) $V_{\text{BE}} = -0.7$ V, $V_{\text{CE}} = -3.83$ V, $V_{\text{CB}} = -3.13$ V
- $I_{\text{B}} = 30 \mu\text{A}$, $I_{\text{E}} = 1.3$ mA, $I_{\text{C}} = 1.27$ mA
- $3 \mu\text{A}$
- 425 mW
- 33.3
- 500 μA , 3.33 μA , 4.03 V
- See Figure ANS-12.
- Open, low resistance
- (a) 27.8 (b) 109
- Q_2 or Q_4 shorted collector to emitter, short from pin 2 of relay to ground, Q_1 or Q_3 open collector to emitter
- (a) 40 V (b) 200 mA dc (c) 625 mW
 (d) 1.5 W (e) 35
- 1.26 W
- (a) Saturated (b) Not saturated

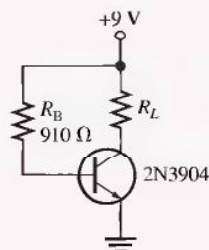


▲ FIGURE ANS-11



▲ FIGURE ANS-12

41. (a) No parameters are exceeded.
 (b) No parameters are exceeded.
 43. Yes, marginally; $V_{CE} = 0.8 \text{ V}$; $I_C = 75 \text{ mA}$
 45. See Figure ANS-13.

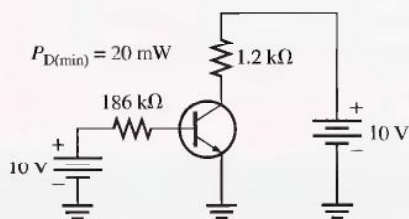


▲ FIGURE ANS-13

47. R_B shorted
 49. Collector-emitter shorted
 51. R_E leaky
 53. R_B open

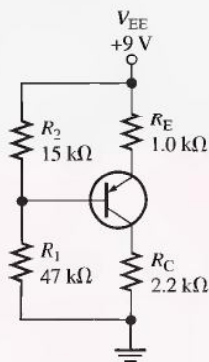
Chapter 5

1. Saturation
 3. 18 mA
 5. $V_{CE} = 20 \text{ V}$; $I_{C(\text{sat})} = 2 \text{ mA}$
 7. See Figure ANS-14.



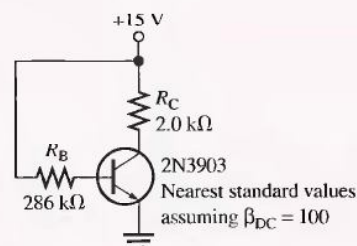
▲ FIGURE ANS-14

9. 69.1
 11. $I_C \cong 809 \mu\text{A}$; $V_{CE} = 13.2 \text{ V}$
 13. See Figure ANS-15.



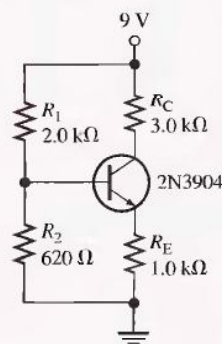
▲ FIGURE ANS-15

15. (a) -1.41 mA , -8.67 V
 (b) 12.2 mW
 17. $I_{CQ} = 92.5 \text{ mA}$; $V_{CEQ} = 2.75 \text{ V}$
 19. 27.7 mA to 69.2 mA; 6.23 V to 2.08 V; Yes
 21. $V_B = -391 \text{ mV}$; $V_E = -1.10 \text{ V}$; $V_C = 3.22 \text{ V}$
 23. 0.09 mA
 25. $I_C = 16.3 \text{ mA}$; $V_{CE} = -6.95 \text{ V}$
 27. 2.53 kΩ
 29. 7.87 mA; 2.56 V
 31. (a) Open collector
 (b) No problems
 (c) Transistor shorted collector-to-emitter
 (d) Open emitter
 33. (a) 1: 10 V, 2: float, 3: -3.59 V , 4: 10 V
 (b) 1: 10 V, 2: 4.05 V, 3: 4.75 V, 4: 4.05 V
 (c) 1: 10 V, 2: 0 V, 3: 0 V, 4: 10 V
 (d) 1: 10 V, 2: 570 mV, 3: 1.27 V, 4: float
 (e) 1: 10 V, 2: 0 V, 3: 0.7 V, 4: 0 V
 (f) 1: 10 V, 2: 0 V, 3: 3.59 V, 4: 10 V
 35. R_1 open, R_2 shorted, BE junction open
 37. $V_C = V_{CC} = 9.1 \text{ V}$, V_B normal, $V_E = 0 \text{ V}$
 39. None are exceeded.
 41. 457 mW
 43. See Figure ANS-16.



▲ FIGURE ANS-16

45. See Figure ANS-17.

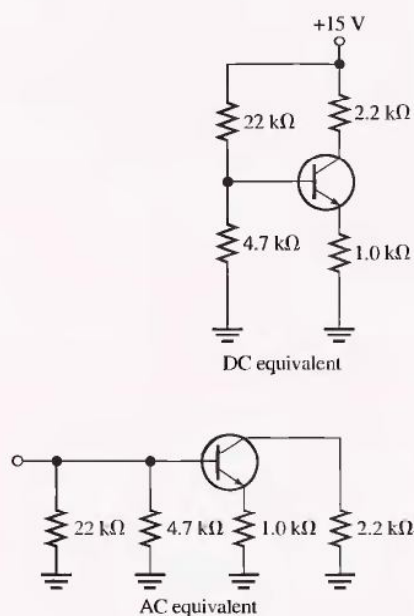


▲ FIGURE ANS-17

47. Yes
49. V_{CEQ} will be less, causing the transistor to saturate at a slightly higher temperature, thus limiting the low temperature response.
51. R_C open
53. R_2 open
55. R_C shorted

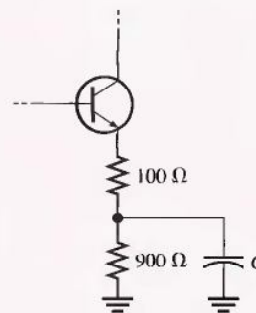
Chapter 6

1. Slightly greater than 1 mA min.
3. 8.33Ω
5. $r'_e \cong 19 \Omega$
7. See Figure ANS-18.



▲ FIGURE ANS-18

9. (a) $1.29 \text{ k}\Omega$ (b) 968Ω (c) 171
11. (a) $V_B = 3.25 \text{ V}$ (b) $V_E = 2.55 \text{ V}$
 (c) $I_E = 2.55 \text{ mA}$ (d) $I_C \cong 2.55 \text{ mA}$
 (e) $V_C = 9.59 \text{ V}$ (f) $V_{CE} = 7.04 \text{ V}$
13. $A'_v = 131$; $\theta = 180^\circ$
15. $A_{v(max)} = 65.5$; $A_{v(min)} = 2.06$
17. A_v is reduced to approximately 30. See Figure ANS-19.
19. $R_{in(tot)} = 3.1 \text{ k}\Omega$; $V_{OUT} = 1.06 \text{ V}$
21. 270Ω
23. 8.8
25. $R_{in(emitter)} = 2.28 \Omega$; $A_v = 526$; $A_f \cong 1$; $A_p = 526$
27. 400

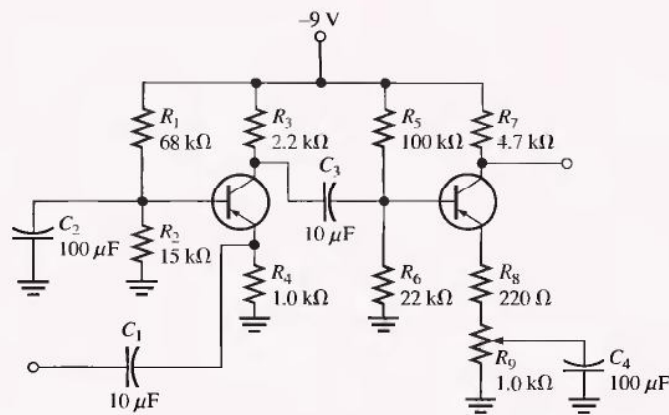


▲ FIGURE ANS-19

29. (a) $A_{v1} = 93.6$, $A_{v2} = 302$
 (b) $A'_v = 28,267$
 (c) $A_{v1(dB)} = 39.4 \text{ dB}$, $A_{v2(dB)} = 49.6 \text{ dB}$, $A'_{v(dB)} = 89.0 \text{ dB}$
31. $V_{B1} = 2.16 \text{ V}$, $V_{E1} = 1.46 \text{ V}$, $V_{C1} \cong 5.16 \text{ V}$, $V_{B2} = 5.16 \text{ V}$,
 $V_{E2} = 4.46 \text{ V}$, $V_{C2} \cong 7.54 \text{ V}$, $A_{v1} = 66$, $A_{v2} = 179$, $A'_v = 11,814$
33. (a) 1.41 (b) 2.00 (c) 3.16 (d) 10.0 (e) 100
35. V_1 : differential output voltage
 V_2 : noninverting input voltage
 V_3 : single-ended output voltage
 V_4 : differential input voltage
 I_1 : bias current
37. (a) Single-ended input; differential output
 (b) Single-ended input; single-ended output
 (c) Differential input; single-ended output
 (d) Differential input; differential output
39. Cutoff, 10 V
- 41.

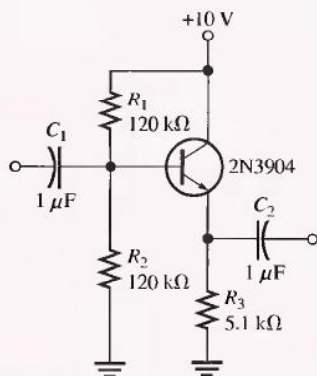
TEST POINT	DC VOLTS	AC VOLTS (RMS)
Input	0 V	$25 \mu\text{V}$
Q_1 base	2.99 V	$20.8 \mu\text{V}$
Q_1 emitter	2.29 V	0 V
Q_1 collector	7.44 V	1.95 mV
Q_2 base	2.99 V	1.95 mV
Q_2 emitter	2.29 V	0 V
Q_2 collector	7.44 V	589 mV
Output	0 V	589 mV

43. (a) $V_C = 5.87 \text{ V}$, $V_e = 850 \text{ mV}$
 (b) $V_C = 5.87 \text{ V}$, $V_e = 0 \text{ V}$
 (c) $V_C = 5.87 \text{ V}$, $V_e = 0 \text{ V}$
 (d) $V_C = 5.87 \text{ V}$, $V_e = 203 \text{ mV}$
 (e) $V_C = 5.87 \text{ V}$, $V_e = 0 \text{ V}$
 (f) $V_C \cong 0 \text{ V}$, $V_e = 0 \text{ V}$



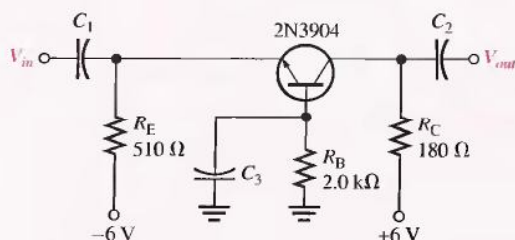
▲ FIGURE ANS-20

45. (a) Q_1 is off (b) 9 V (c) 5.87 V
 47. (a) 700 (b) 40 Ω (c) 20 k Ω
 49. A leaky coupling capacitor affects the bias voltages and attenuates the ac voltage.
 51. See Figure ANS-20.
 53. See Figure ANS-21.



▲ FIGURE ANS-21

55. See Figure ANS-22.

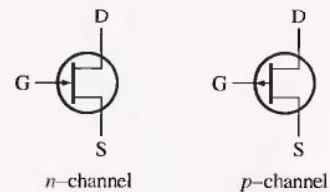


▲ FIGURE ANS-22

57. $A_v = R_C/r'_e$
 $A_v \cong (V_{RC}/I_C)/(0.025 \text{ V}/I_C) = V_{RC}/0.025 = 40V_{RC}$
 59. C_2 shorted
 61. C_1 open
 63. C_3 open

Chapter 7

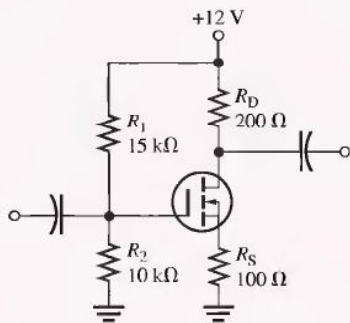
1. (a) Narrows (b) Increases
 3. See Figure ANS-23.



▲ FIGURE ANS-23

5. 5 V
 7. 10 mA
 9. 4 V
 11. -2.63 V
 13. $g_m = 1429 \mu\text{S}$, $y_{fs} = 1429 \mu\text{S}$
 15. $V_{GS} = 0 \text{ V}$, $I_D = 8 \text{ mA}$
 $V_{GS} = -1 \text{ V}$, $I_D = 5.12 \text{ mA}$
 $V_{GS} = -2 \text{ V}$, $I_D = 2.88 \text{ mA}$
 $V_{GS} = -3 \text{ V}$, $I_D = 1.28 \text{ mA}$
 $V_{GS} = -4 \text{ V}$, $I_D = 0.320 \text{ mA}$
 $V_{GS} = -5 \text{ V}$, $I_D = 0 \text{ mA}$
 17. 800 Ω
 19. (a) 20 mA (b) 0 A (c) Increases
 21. 211 Ω
 23. 9.80 M Ω

25. $I_D \cong 5.3 \text{ mA}$, $V_{GS} \cong 2.1 \text{ V}$
 27. $I_D \cong 1.9 \text{ mA}$, $V_{GS} \cong -1.5 \text{ V}$
 29. The enhancement mode
 31. The gate is insulated from the channel.
 33. 4.69 mA
 35. (a) Depletion (b) Enhancement
 (c) Zero bias (d) Depletion
 37. (a) 4 V (b) 5.4 V (c) -4.52 V
 39. (a) 5 V, 3.18 mA (b) 3.2 V, 1.02 mA
 41. R_D or R_S open, JFET open D-to-S, $V_{DD} = 0 \text{ V}$, or ground connection open.
 43. No change
 45. The $1.0 \text{ M}\Omega$ bias resistor is open.
 47. $V_{OUT} = 300 \text{ mV}$ for $\text{pH} = 5$; $V_{OUT} = -400 \text{ mV}$ for $\text{pH} = 9$
 49. $V_{OUT} = +12.1 \text{ V}$ assuming typical values.
 51. (a) -0.5 V (b) 25 V (c) 310 mW (d) -25 V
 53. $2000 \mu\text{S}$
 55. 1 V
 57. $I_D \cong 13 \text{ mA}$ when $V_{GS} = +3 \text{ V}$, $I_D \cong 0.4 \text{ mA}$ when $V_{GS} = -2 \text{ V}$.
 59. -3.0 V
 61. $I_D = 3.58 \text{ mA}$; $V_{GS} = -4.21 \text{ V}$
 63. 6.01 V
 65. See Figure ANS-24.



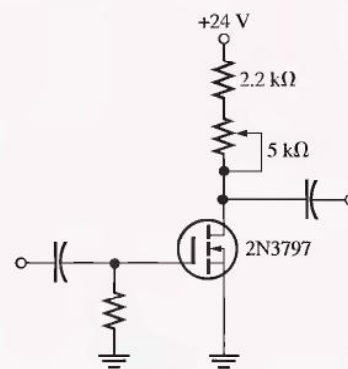
▲ FIGURE ANS-24

67. R_D shorted
 69. R_1 open
 71. R_D open
 73. Drain-source shorted

Chapter 8

1. (a) $60 \mu\text{A}$ (b) $900 \mu\text{A}$ (c) 3.6 mA (d) 6 mA
 3. 14.2
 5. (a) n -channel D-MOSFET with zero-bias; $V_{GS} = 0$
 (b) p -channel JFET with self-bias; $V_{GS} = -0.99 \text{ V}$
 (c) n -channel E-MOSFET with voltage-divider bias; $V_{GS} = 3.84 \text{ V}$

7. (a) n -channel D-MOSFET
 (b) n -channel JFET
 (c) p -channel E-MOSFET
 9. Figure 8-18(b): approximately 4 mA
 Figure 8-18(c): approximately 3.2 mA
 11. 920 mV
 13. (a) 4.32 (b) 9.92
 15. $\approx 7.5 \text{ mA}$
 17. 2.54
 19. 33.6 mV rms
 21. $9.84 \text{ M}\Omega$
 23. $V_{GS} = 9 \text{ V}$; $I_D = 3.13 \text{ mA}$; $V_{DS} = 13.3 \text{ V}$; $V_{ds} = 675 \text{ mV}$
 25. $R_{in} \cong 10 \text{ M}\Omega$; $A_v = 0.783$
 27. (a) 0.906 (b) 0.299
 29. 250Ω
 31. (a) $V_{D1} = V_{DD}$; no Q_1 drain signal; no output signal
 (b) $V_{D1} \cong 0 \text{ V}$ (floating); no Q_1 drain signal; no output signal
 (c) $V_{GS1} = 0 \text{ V}$; $V_S = 0 \text{ V}$; V_{D1} less than normal; clipped output signal
 (d) Correct signal at Q_1 drain; no Q_1 gate signal; no output signal
 (e) $V_{D2} = V_{DD}$; correct signal at Q_2 gate; no Q_2 drain signal or output signal
 33. The $10 \mu\text{F}$ capacitor between Q_1 drain and Q_2 gate is open.
 35. $V_{DC} = 4.35 \text{ V}$; $V_{ac} = 1.29 \text{ V rms}$
 37. (a) -3.0 V (b) 20 V dc
 (c) 200 mW (d) $\pm 10 \text{ V dc}$
 39. $900 \mu\text{S}$
 41. 1.5 mA
 43. 2.0; 6.82
 45. See Figure ANS-25.

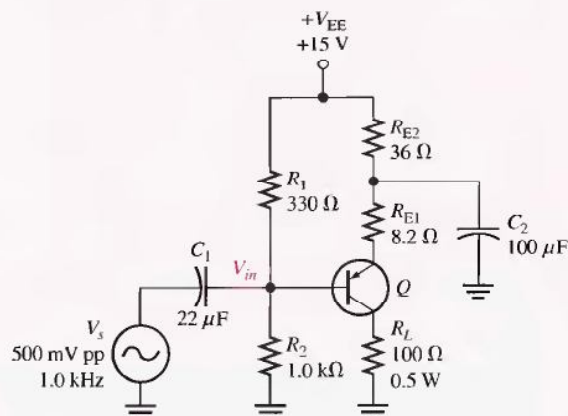


▲ FIGURE ANS-25

47. C_2 open
 49. R_S shorted
 51. R_1 open
 53. R_2 open

Chapter 9

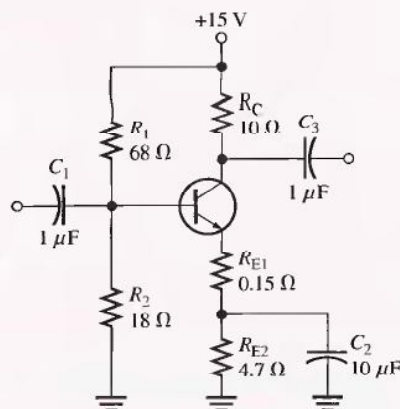
1. (a) $I_{CQ} = 68.4 \text{ mA}$; $V_{CEQ} = 5.14 \text{ V}$
(b) $A_v = 11.7$; $A_p = 263$
3. The changes are shown on Figure ANS-26. The advantage of this arrangement is that the load resistor is referenced to ground.



▲ FIGURE ANS-26

5. For Figure 9-42(a): 39.8 mA, 1.99 V; For Figure 9-42(b): 12.3 mA, 2.88 V
7. 265 mW
9. (a) $V_{B(Q1)} = +0.7 \text{ V}$; $V_{B(Q2)} = -0.7 \text{ V}$; $V_E = 0 \text{ V}$;
 $V_{CEQ(Q1)} = +9 \text{ V}$; $V_{CEQ(Q2)} = -9 \text{ V}$; $I_{CQ} = 8.3 \text{ mA}$
(b) $P_L = 0.5 \text{ W}$
11. (a) $V_{B(Q1)} = +8.2 \text{ V}$; $V_{B(Q2)} = +6.8 \text{ V}$;
 $V_E = +7.5 \text{ V}$; $I_{CQ} = 6.8 \text{ mA}$;
 $V_{CEQ(Q1)} = +7.5 \text{ V}$;
 $V_{CEQ(Q2)} = -7.5 \text{ V}$
(b) $P_L = 167 \text{ mW}$
13. (a) C_2 open or Q_2 open
(b) Power supply off, open R_1 , Q_1 base shorted to ground
(c) Q_1 has collector-to-emitter short
(d) One or both diodes shorted
15. 450 μW
17. 24 V
19. Negative half of input cycle
21. (a) No dc supply voltage or R_1 open
(b) D_1 or D_2 open
(c) No fault
(d) Q_1 shorted C-to-E
23. 6 V dc, positive alternation of input signal
25. C_1 is connected backwards.
27. 51 W
29. Gain decreases.
31. T_C is much closer to the actual junction temperature than T_A . In a given operating environment, T_A is always less than T_C .

33. See Figure ANS-27.



▲ FIGURE ANS-27

35. C_m open
37. Q_1 collector-emitter open
39. Q_2 drain-source open

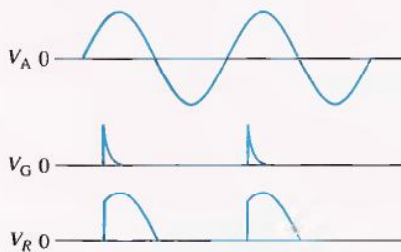
Chapter 10

1. If $C_1 = C_2$, the critical frequencies are equal, and they will both cause the gain to drop at 40 dB/decade below f_c .
3. BJT: C_{be} , C_{bc} , C_{ce} ; FET: C_{gs} , C_{gd} , C_{ds}
5. 812 pF
7. $C_{in(miller)} = 6.95 \text{ pF}$; $C_{out(miller)} = 5.28 \text{ pF}$
9. 24 mV rms; 34 dB
11. (a) 3.01 dBm (b) 0 dBm (c) 6.02 dBm
(d) -6.02 dBm
13. (a) 318 Hz (b) 1.59 kHz
15. At $0.1f_c$: $A_v = 18.8 \text{ dB}$
At f_c : $A_v = 35.8 \text{ dB}$
At $10f_c$: $A_v = 38.8 \text{ dB}$
17. Input RC circuit: $f_c = 3.34 \text{ Hz}$
Output RC circuit: $f_c = 3.01 \text{ kHz}$
Output f_c is dominant.
19. Input circuit: $f_c = 4.32 \text{ MHz}$
Output circuit: $f_c = 94.9 \text{ MHz}$
Input f_c is dominant.
21. Input circuit: $f_c = 12.9 \text{ MHz}$
Output circuit: $f_c = 54.5 \text{ MHz}$
Input f_c is dominant.
23. $f_{cl} = 136 \text{ Hz}$, $f_{cu} = 8 \text{ kHz}$
25. $BW = 5.26 \text{ MHz}$, $f_{cu} \approx 5.26 \text{ MHz}$
27. 230 Hz; 1.2 MHz
29. 514 kHz
31. $\approx 2.5 \text{ MHz}$
33. Increase the frequency until the output voltage drops to 3.54 V rms. This is f_{cu} .

35. 23.1 Hz
 37. No effect
 39. 112 pF
 41. $C_{gd} = 1.3 \text{ pF}$; $C_{gs} = 3.7 \text{ pF}$; $C_{ds} = 3.7 \text{ pF}$
 43. $\approx 10.5 \text{ MHz}$
 45. R_C open
 47. R_2 open

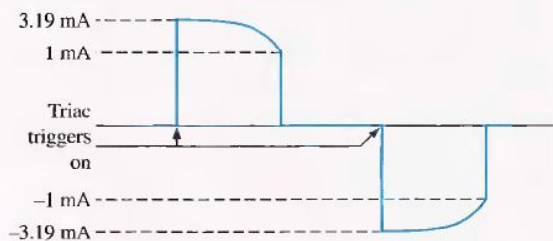
Chapter 11

1. $I_A = 24.1 \text{ mA}$
 3. See "Turning the SCR On" in Section 11-2.
 5. Add a transistor to provide inversion of negative half-cycle in order to obtain a positive gate trigger.
 7. See Figure ANS-28.



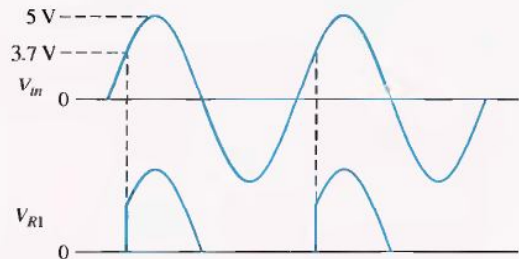
▲ FIGURE ANS-28

9. See Figure ANS-29.



▲ FIGURE ANS-29

11. Anode, cathode, anode gate, cathode gate
 13. 6.48 V
 15. (a) 9.79 V (b) 5.2 V
 17. See Figure ANS-30.

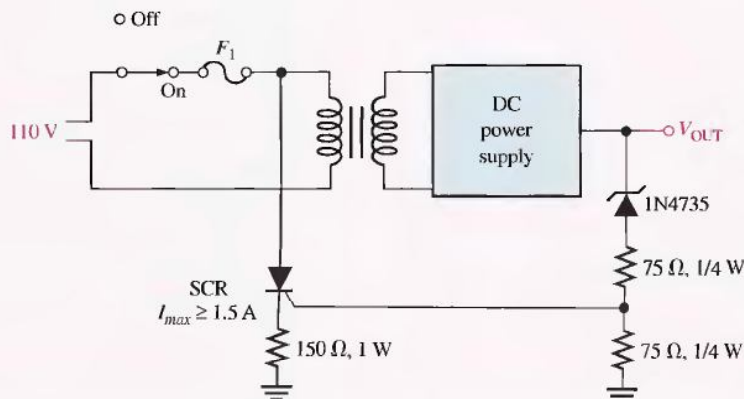


▲ FIGURE ANS-30

19. The parasitic transistor turns on and the device acts as a thyristor.
 21. (a) 12 V (b) 0 V
 23. When the switch is closed, the battery V_2 causes illumination of the lamp. The light energy causes the LASCR to conduct and thus energize the relay. When the relay is energized, the contacts close and 115 V ac are applied to the motor.
 25. 30 mA
 27. Reflected
 29. 0 V
 31. As the PUT gate voltage increases, the PUT triggers on later to the ac cycle causing the SCR to fire later in the cycle, conduct for a shorter time, and decrease power to the motor.
 33. See Figure ANS-31.
 35. Cathode-anode shorted
 37. R_1 shorted

Chapter 12

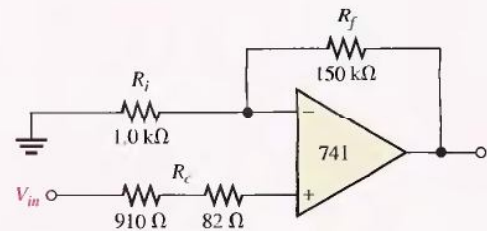
1. *Practical op-amp*: High open-loop gain, high input impedance, low output impedance, high CMRR.
Ideal op-amp: Infinite open-loop gain, infinite input impedance, zero output impedance, infinite CMRR.



▲ FIGURE ANS-31

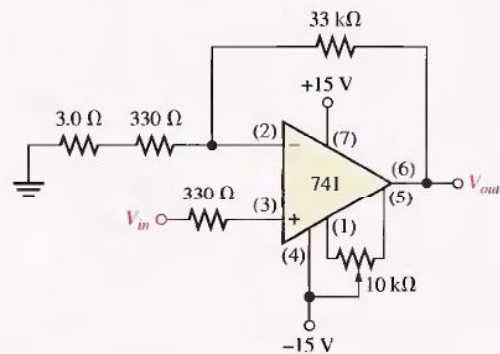
3. (a) Single-ended input
(b) Differential input
(c) Common-mode input
5. 120 dB
7. $8.1 \mu\text{A}$
9. $1.6 \text{ V}/\mu\text{s}$
11. (a) Voltage-follower
(b) Noninverting
(c) Inverting
13. (a) $A_{cl(NI)} = 374$
(b) $V_{out} = 3.74 \text{ V rms}$
(c) $V_f = 9.99 \text{ mV rms}$
15. (a) $49 \text{ k}\Omega$
(b) $3 \text{ M}\Omega$
(c) $84 \text{ k}\Omega$
(d) $165 \text{ k}\Omega$
17. (a) 10 mV , in phase
(b) -10 mV , 180° out of phase
(c) 223 mV , in phase
(d) -100 mV , 180° out of phase
19. (a) $Z_{in(NI)} = 8.41 \text{ G}\Omega$; $Z_{out(NI)} = 89.2 \text{ m}\Omega$
(b) $Z_{in(NI)} = 6.20 \text{ G}\Omega$; $Z_{out(NI)} = 4.04 \text{ m}\Omega$
(c) $Z_{in(NI)} = 5.30 \text{ G}\Omega$; $Z_{out(NI)} = 19.0 \text{ m}\Omega$
21. (a) $Z_{in(I)} = 10 \text{ k}\Omega$; $Z_{out(I)} = 5.12 \text{ m}\Omega$
(b) $Z_{in(I)} = 100 \text{ k}\Omega$; $Z_{out(I)} = 7.41 \text{ m}\Omega$
(c) $Z_{in(I)} = 470 \Omega$; $Z_{out(I)} = 6.22 \text{ m}\Omega$
23. (a) $2.69 \text{ k}\Omega$ (b) $1.45 \text{ k}\Omega$ (c) $53 \text{ k}\Omega$
 R_c is placed between V_{in} and the + input
25. 175 nV
27. $A_v = 125,892$; $BW_{ol} = 200 \text{ Hz}$
29. (a) 0.997 (b) 0.923 (c) 0.707
(d) 0.515 (e) 0.119
31. (a) -51.5° (b) -7.17° (c) -85.5°
33. (a) 90 dB (b) -281°
35. (a) 29.8 dB (b) 23.9 dB (c) 0 dB
All are closed-loop gains.
37. 71.7 dB
39. (a) $A_{cl(VF)} = 1$; $BW = 2.8 \text{ MHz}$
(b) $A_{cl(I)} = -45.5$; $BW = 61.6 \text{ kHz}$
(c) $A_{cl(NI)} = 13$; $BW = 215 \text{ kHz}$
(d) $A_{cl(I)} = -179$; $BW = 15.7 \text{ kHz}$
41. (a) Faulty op-amp or R_1 open
(b) R_2 open, forcing open-loop operation
43. The gain becomes a fixed -100 , with no effect as the gain potentiometer is adjusted.
45. Op-amp gain will be ten times too high.
47. $Z_{in(NI)} = 3.96 \text{ G}\Omega$
49. 50,000

51. See Figure ANS-32.



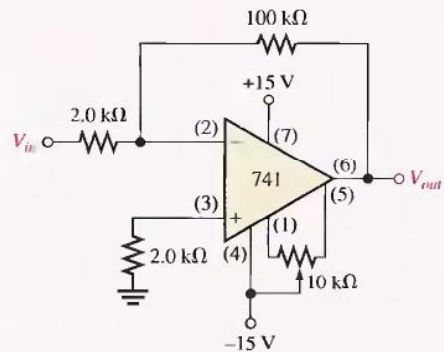
▲ FIGURE ANS-32

53. See Figure ANS-33.



▲ FIGURE ANS-33

55. See Figure ANS-34.

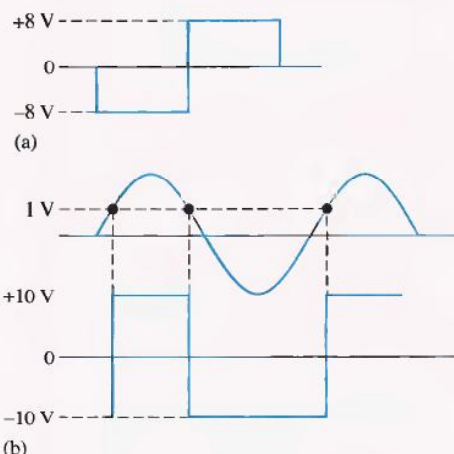


▲ FIGURE ANS-34

57. R_f open
59. R_f leaky
61. R_f shorted
63. R_f leaky
65. R_i shorted
67. R_f open
69. R_f open
71. R_i open

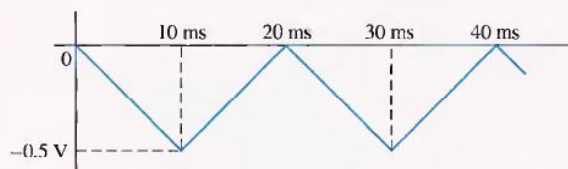
Chapter 13

1. 24 V, with distortion
3. $V_{UTP} = +2.77$ V, $V_{LTP} = -2.77$ V
5. See Figure ANS-35.



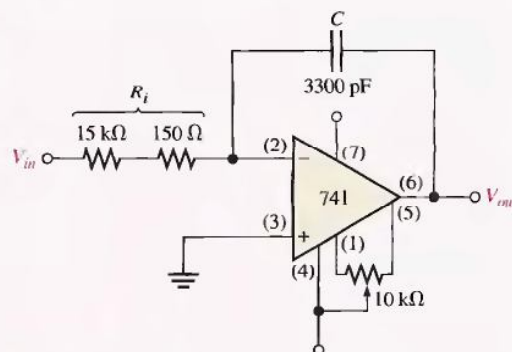
▲ FIGURE ANS-35

7. +8.57 V and -0.968 V
9. (a) -2.5 V (b) -3.52 V
11. 110 k Ω
13. $V_{OUT} = -3.57$ V, $I_f = 357$ μ A
15. -4.06 mV/ μ s
17. 1 mA
19. See Figure ANS-36.



▲ FIGURE ANS-36

21. Output not correct; R_2 is open.
23. 50 k Ω resistor open
25. The output of IC2 will saturate positively.
27. +8 V
29. $f_m = 100$ kHz. See Figure ANS-37.
31. Op-amp inputs shorted together
33. D_1 shorted
35. Middle 10 k Ω resistor shorted
37. R_f open
39. C open



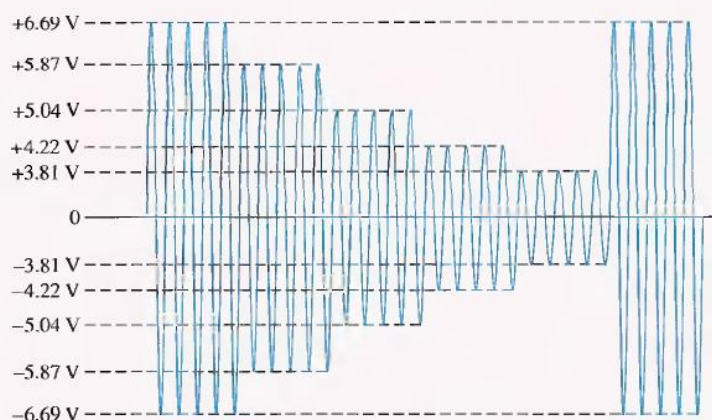
▲ FIGURE ANS-37

Chapter 14

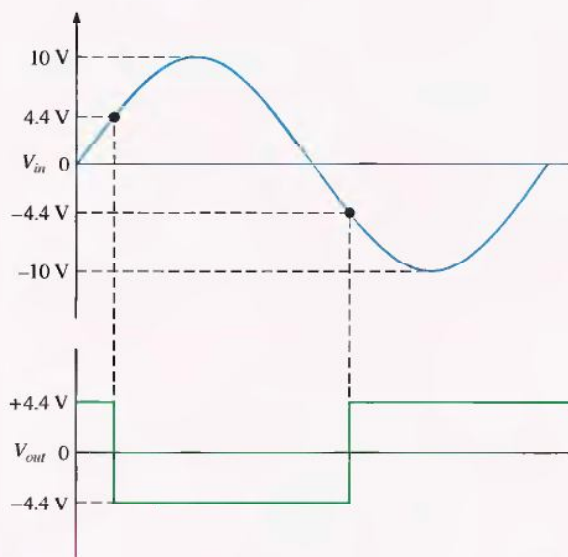
1. $A_{v(1)} = A_{v(2)} = 101$
3. 1.005 V
5. 51.5
7. Change R_G to 2.2 k Ω .
9. 300
11. Change the 18 k Ω resistor to 23.2 k Ω .
13. Connect pin 6 directly to pin 10, and connect pin 14 directly to pin 15 to make $R_f = 0$.
15. 500 μ A, 5 V
17. $A_v \approx 11.6$
19. See Figure ANS-38.
21. See Figure ANS-39.
23. (a) -0.301 (b) 0.301 (c) 1.70 (d) 2.11
25. The output of a log amplifier is limited to 0.7 V because of the transistor's pn junction.
27. -157 mV
29. $V_{out(max)} = -147$ mV, $V_{out(min)} = -89.2$ mV; the 1 V input peak is reduced 85% whereas the 100 mV input peak is reduced only 10%.
31. See Figure ANS-40.
33. TP1: ≈ 0 V
TP2: ≈ 0 V
TP3: 21.2 mV @ 1 kHz
TP4: +15 V
TP5: 0 V
35. R open
37. Zener diode open

Chapter 15

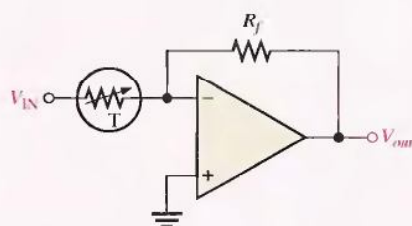
1. (a) Band-pass (b) High-pass (c) Low-pass (d) Band-stop
3. 48.2 kHz, No
5. 700 Hz, 5.04



▲ FIGURE ANS-38



▲ FIGURE ANS-39



▲ FIGURE ANS-40

7. (a) 1, not Butterworth
 (b) 1.44, approximate Butterworth
 (c) 1st stage: 1.67; 2nd stage: 1.67; Not Butterworth
9. (a) Chebyshev (b) Butterworth
 (c) Bessel (d) Butterworth

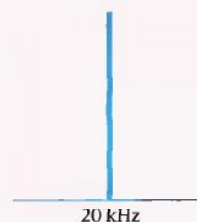
11. 190 Hz
13. Add another identical stage and change the ratio of the feedback resistors to 0.068 for first stage, 0.586 for second stage, and 1.482 for third stage.
15. Exchange positions of resistors and capacitors.
17. (a) Decrease R_1 and R_2 or C_1 and C_2 .
 (b) Increase R_3 or decrease R_4 .
19. (a) $f_0 = 4.95$ kHz, $BW = 3.84$ kHz
 (b) $f_0 = 449$ Hz, $BW = 96.4$ Hz
 (c) $f_0 = 15.9$ kHz, $BW = 838$ Hz
21. Sum the low-pass and high-pass outputs with a two-input adder.
23. R_4 shorted
25. C_3 shorted
27. R_1 open
29. R_1 open
31. R_7 open

Chapter 16

1. An oscillator requires no input (other than dc power).
3. $\frac{1}{75} = 0.0133$
5. 733 mV
7. 50 k Ω
9. 2.34 k Ω
11. 136 k Ω , 628 Hz
13. 10
15. Change R_1 to 3.54 k Ω
17. $R_4 = 65.8$ k Ω , $R_3 = 47$ k Ω
19. 3.33 V, 6.67 V
21. 0.0076 μ F
23. Drain-to-source shorted
25. Collector-to-emitter shorted
27. R_2 open

Chapter 17

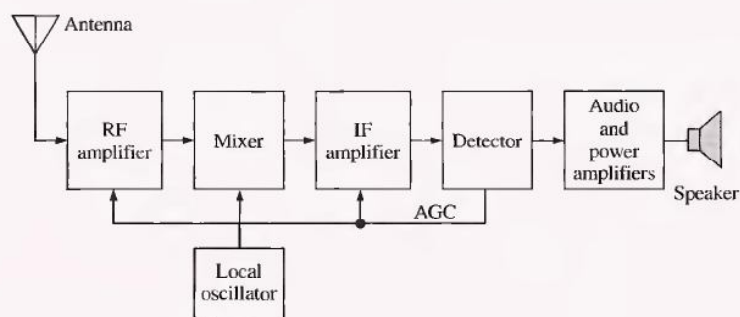
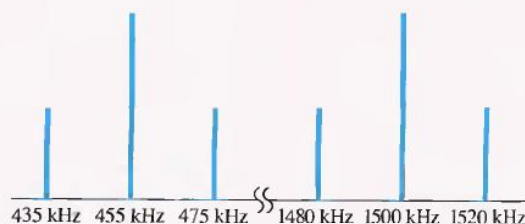
1. See Figure ANS-41.
3. 1135 kHz
5. $f_{RF} = 91.2 \text{ MHz}$; $f_{IF} = 10.7 \text{ MHz}$
7. $739 \mu\text{A}$
9. -8.12 V
11. (a) $+0.28 \text{ V}$ (b) $+1.024 \text{ V}$
(c) $+2.07 \text{ V}$ (d) $+2.49 \text{ V}$
13. $f_{diff} = 8 \text{ kHz}$; $f_{sum} = 10 \text{ kHz}$
15. $f_{diff} = 1.7 \text{ MHz}$; $f_{sum} = 1.9 \text{ MHz}$; $f_c = 1.8 \text{ MHz}$
17. $f_c = 850 \text{ kHz}$; $f_m = 3 \text{ kHz}$
19. $V_{out} = 15 \text{ mV} \cos[2\pi (1100 \text{ kHz})t] - 15 \text{ mV} \cos[2\pi (5500 \text{ kHz})t]$
21. See Figure ANS-42.
23. See Figure ANS-43.
25. 450 kHz–460 kHz: IF amplifier; 10 Hz–5 kHz: Audio/Power amplifiers
27. The modulating input signal is applied to the control voltage terminal of the VCO. As the input signal amplitude varies, the output frequency of the VCO varies proportionately.
29. Varactor

**▲ FIGURE ANS-43**

31. (a) 10 MHz (b) 48.3 mV
33. 1005 Hz
35. $f_o = 233 \text{ kHz}$; $f_{lock} = \pm 104 \text{ kHz}$; $f_{cap} = \pm 4.56 \text{ kHz}$

Chapter 18

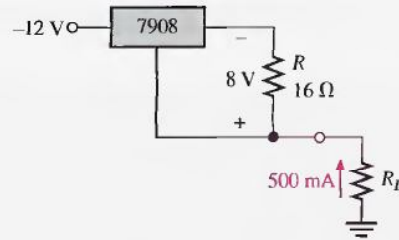
1. 0.0333%
3. 1.01%
5. A: Reference voltage, B: Control element, C: Error detector, D: Sampling circuit
7. 8.51 V
9. 9.57 V
11. 500 mA

**▲ FIGURE ANS-41****▲ FIGURE ANS-42**

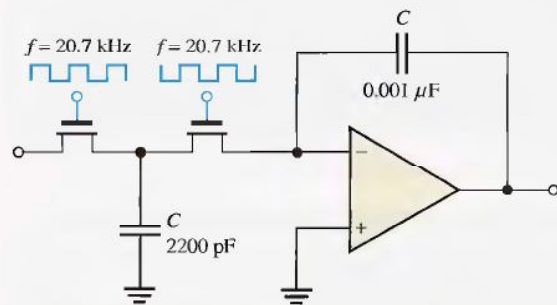
13. 10 mA
15. $I_{L(\max)} = 250 \text{ mA}$, $P_{Rl} = 6.25 \text{ W}$
17. 40%
19. V_{OUT} decreases
21. 14.3 V
23. 1.3 mA
25. 2.8Ω
27. $R_{\text{limit}} = 0.35 \Omega$
29. See Figure ANS-44.
31. R_2 leaky
33. Q_2 collector-to-emitter open

Chapter 19

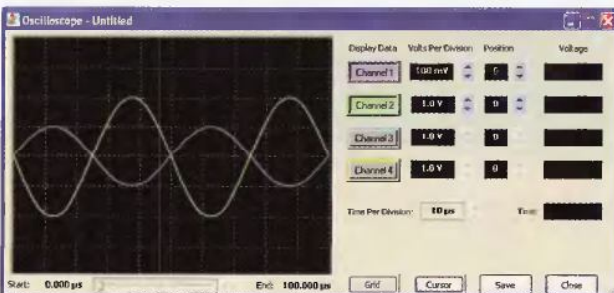
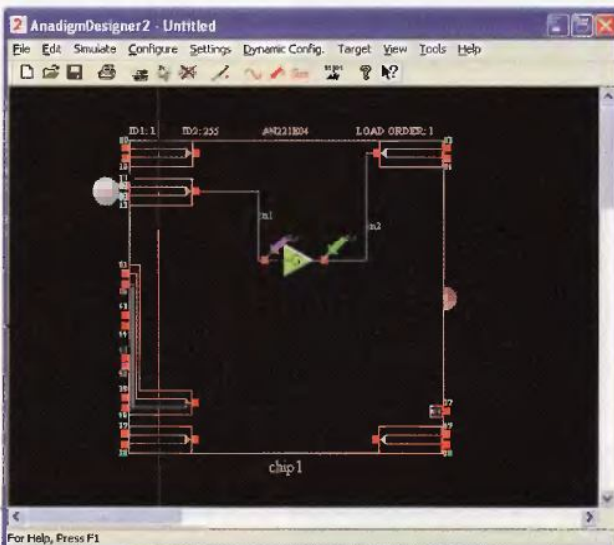
1. 4.55 k Ω
3. $f = 20.7 \text{ kHz}$. See Figure ANS-45.
5. 606 Ω
7. See Figure ANS-46.
9. See Figure ANS-47.
11. See Figure ANS-48.
13. See Figure ANS-49.



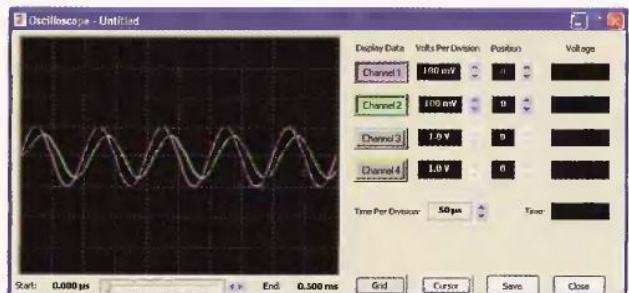
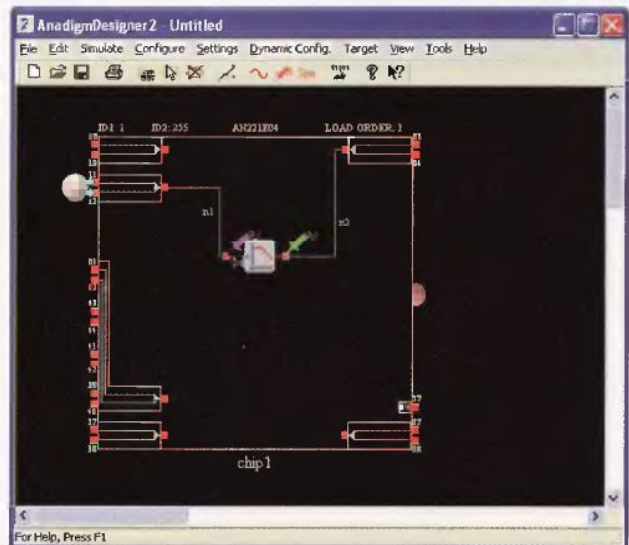
▲ FIGURE ANS-44



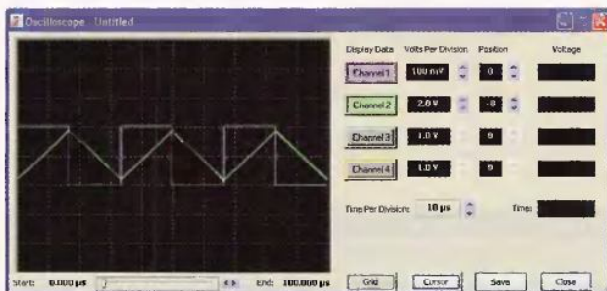
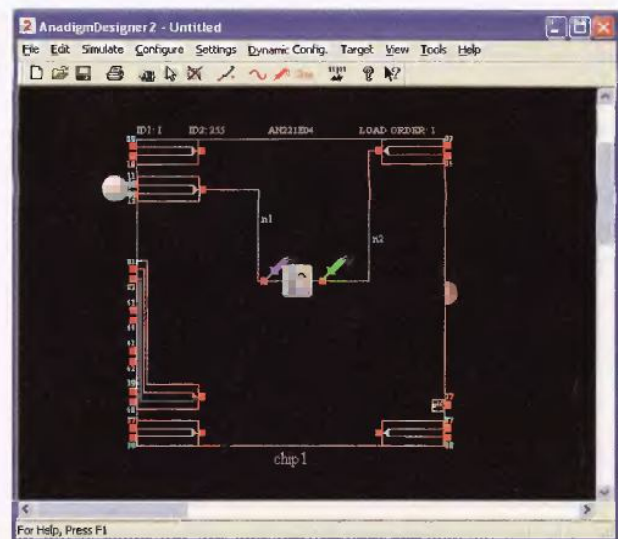
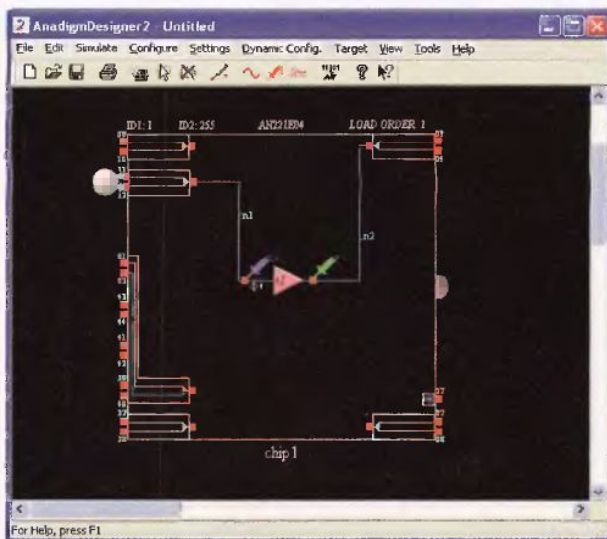
▲ FIGURE ANS-45



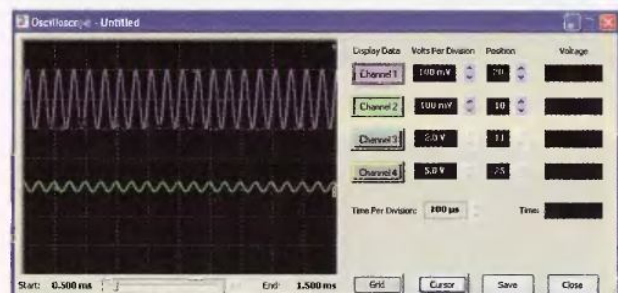
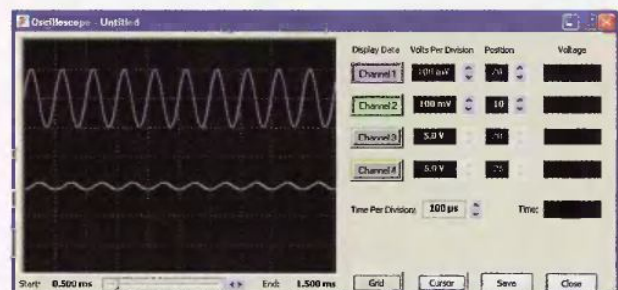
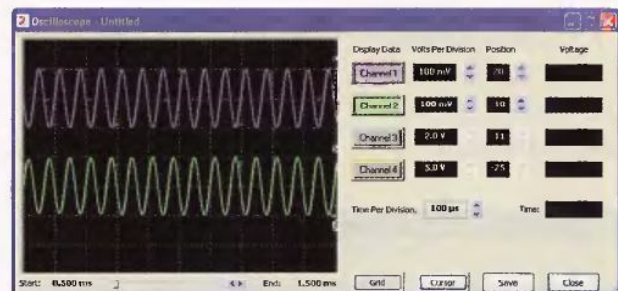
▲ FIGURE ANS-46



▲ FIGURE ANS-47



▲ FIGURE ANS-48



▲ FIGURE ANS-49

Glossary

ac ground A point in a circuit that appears as ground to ac signals only.

active filter A frequency-selective circuit consisting of active devices such as transistors or op-amps coupled with reactive components.

A/D conversion A process whereby information in analog form is converted into digital form.

alpha (α) The ratio of dc collector current to dc emitter current in a bipolar junction transistor.

amplification The process of increasing the power, voltage, or current by electronic means.

amplifier An electronic circuit having the capability to amplify power, voltage, or current.

amplitude modulation (AM) A communication method in which a lower-frequency signal modulates (varies) the amplitude of a higher-frequency signal (carrier).

analog Characterized by a linear process in which a variable takes on a continuous set of values.

angle of incidence The angle at which a light ray strikes a surface.

anode The *p* region of a diode.

antilogarithm The result obtained when the base of a number is raised to a power equal to the logarithm of that number.

astable Characterized by having no stable states.

atom The smallest particle of an element that possesses the unique characteristics of that element.

atomic number The number of protons in an atom.

attenuation The reduction in the level of power, current, or voltage.

audio Related to the frequency range of sound waves that can be heard by the human ear and generally considered to be in the 20 Hz to 20 kHz range.

avalanche The rapid buildup of conduction electrons due to excessive reverse-bias voltage.

avalanche breakdown The higher voltage breakdown in a zener diode.

balanced modulation A form of amplitude modulation in which the carrier is suppressed; sometimes known as *suppressed-carrier modulation*.

band-pass filter A type of filter that passes a range of frequencies lying between a certain lower frequency and a certain higher frequency.

band-stop filter A type of filter that blocks or rejects a range of frequencies lying between a certain lower frequency and a certain higher frequency.

bandwidth The characteristic of certain types of electronic circuits that specifies the usable range of frequencies that pass from input to output.

barrier potential The amount of energy required to produce full conduction across the *pn* junction in forward bias.

base One of the semiconductor regions in a BJT. The base is very thin and lightly doped compared to the other regions.

Bessel A type of filter response having a linear phase characteristic and less than -20 dB/decade/pole rolloff.

beta (β) The ratio of dc collector current to dc base current in a BJT; current gain from base to collector.

bias The application of a dc voltage to a diode, transistor, or other device to produce a desired mode of operation.

bipolar Characterized by both free electrons and holes as current carriers.

BJT Bipolar junction transistor; a transistor constructed with three doped semiconductor regions separated by two *pn* junctions.

Bode plot An idealized graph of the gain in dB versus frequency used to graphically illustrate the response of an amplifier or filter.

bounding The process of limiting the output range of an amplifier or other circuit.

breakdown The phenomenon of a sudden and drastic increase when a certain voltage is reached across a device.

bridge rectifier A type of full-wave rectifier consisting of diodes arranged in a four-cornered configuration.

Butterworth A type of filter response characterized by flatness in the passband and a -20 dB/decade/pole roll-off.

bypass capacitor A capacitor placed across the emitter resistor of an amplifier.

byte A group of eight bits in binary data.

CAB Configurable analog block; one of the programmable resources in an FPAA generally consisting of one or more op-amps, a switch matrix, and a capacitor bank.

CAM Configurable analog module; a predesigned analog circuit for which some of its parameters can be selectively programmed.

capture range The range of frequencies over which a PLL can acquire lock.

carbon A semiconductive material.

carrier The high radio frequency (RF) signal that carries modulated information in AM, FM, or other systems.

cascade An arrangement of circuits in which the output of one circuit becomes the input to the next.

cathode The *n* region of a diode.

C code A code used for dynamically configuring an FPAA.

center-tapped rectifier A type of full-wave rectifier consisting of a center-tapped transformer and two diodes.

channel The conductive path between the drain and source in a FET.

Chebyshev A type of filter response characterized by ripples in the passband and a greater than -20 dB/decade/pole roll-off.

clamper A circuit that adds a dc level to an ac voltage using a diode and a capacitor.

class A A type of amplifier that operates entirely in its linear (active) region.

class AB A type of amplifier that is biased into slight conduction.

class B A type of amplifier that operates in the linear region for 180° of the input cycle because it is biased at cutoff.

class C A type of amplifier that operates only for a small portion of the input cycle.

clipper See Limiter.

closed-loop An op-amp configuration in which the output is connected back to the input through a feedback circuit.

closed-loop voltage gain (A_{cl}) The voltage gain of an op-amp with external feedback.

CMRR Common-mode rejection ratio; the ratio of open-loop gain to common-mode gain; a measure of an op-amp's ability to reject common-mode signals.

coherent light Light having only one wavelength.

collector The largest of the three semiconductor regions of a BJT.

common-base (CB) A BJT amplifier configuration in which the base is the common terminal to an ac signal or ground.

common-collector (CC) A BJT amplifier configuration in which the collector is the common terminal to an ac signal or ground.

common-drain (CD) A FET amplifier configuration in which the drain is the grounded terminal.

common-emitter (CE) A BJT amplifier configuration in which the emitter is the common terminal to an ac signal or ground.

common-gate (CG) A FET amplifier configuration in which the gate is the grounded terminal.

common mode A condition where two signals applied to differential inputs are of the same phase, frequency, and amplitude.

common-source (CS) A FET amplifier configuration in which the source is the grounded terminal.

comparator A circuit which compares two input voltages and produces an output in either of two states indicating the greater or less than relationship of the inputs.

complementary symmetry transistors Two transistors, one *npn*, and one *pn*, having matched characteristics.

conduction electron A free electron.

conductor A material that conducts electrical current very well.

configuration RAM A random-access memory used in FPAA's for storing configuration data from the shadow RAM immediately prior to reconfiguring the FPAA.

core The central part of an atom, includes the nucleus and all but the valence electrons.

covalent Related to the bonding of two or more atoms by the interaction of their valence electrons.

critical angle The angle that defines whether a light ray will be reflected or refracted when it strikes a surface.

critical frequency The frequency at which the response of an amplifier or filter is 3 dB less than at midrange.

crossover distortion Distortion in the output of a class B push-pull amplifier at the point where each transistor changes from the cutoff state to the *on* state.

crystal A solid material in which the atoms are arranged in a symmetrical pattern.

current The rate of flow of electrical charge.

current mirror A circuit that uses matching diode junctions to form a current source. The current in a diode junction is reflected as a matching current in the other junction (which is typically the base-emitter junction of a transistor). Current mirrors are commonly used to bias a push-pull amplifier.

cutoff The nonconducting state of a transistor.

cutoff frequency Another term for critical frequency.

cutoff voltage The value of the gate-to-source voltage that makes the drain current approximately zero.

D/A conversion The process of converting a sequence of digital codes to an analog form.

damping factor A filter characteristic that determines the type of response.

dark current The amount of thermally generated reverse current in a photodiode in the absence of light.

darlington pair A configuration of two transistors in which the collectors are connected and the emitter of the first drives the base of the second to achieve beta multiplication.

dBm A unit for measuring power levels referenced to 1 mW.

dc load line A straight line plot of I_C and V_{CE} for a transistor circuit.

decade A ten-times increase or decrease in the value of a quantity such as frequency.

decibel (dB) A logarithmic measure of the ratio of one power to another or one voltage to another.

demodulation The process in which the information signal is recovered from the IF carrier signal; the reverse of modulation.

depletion In a MOSFET, the process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.

depletion region The area near a *pn* junction on both sides that has no majority carriers.

derivative The instantaneous rate of change of a function, determined mathematically.

development software A software that is used for entering a circuit design on the computer, simulating the design, and downloading the design to the FPAA device.

diac A two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction when properly activated.

differential mode A mode of op-amp operation in which two opposite polarity signal voltages are applied to two inputs.

differential amplifier (diff-amp) An amplifier in which the output is a function of the difference between two input voltages, used as the input stage of an op-amp.

differentiator A circuit that produces an output which approximates the instantaneous rate of change of the input function.

digital Characterized by a process in which a variable takes on either of two values.

diode A semiconductor device with a single *pn* junction that conducts current in only one direction.

diode drop The voltage across the diode when it is forward-biased; approximately the same as the barrier potential and typically 0.7 V for silicon.

discriminator A type of FM demodulator.

doping The process of imparting impurities to an intrinsic semiconductive material in order to control its conduction characteristics.

downloading The process of implementing the software description of a circuit in an FPAA.

drain One of the three terminals of a FET analogous to the collector of a BJT.

dynamic reconfiguration The process of downloading a design modification or new design in an FPAA while it is operating in a system without the need to power down or reset the system; also known as "on-the-fly" reprogramming.

dynamic resistance The nonlinear internal resistance of a semiconductive material.

efficiency The ratio of the signal power delivered to a load to the power from the power supply of an amplifier.

electroluminescence The process of releasing light energy by the recombination of electrons in a semiconductor.

electrostatic discharge (ESD) The discharge of a high voltage through an insulating path that can destroy an electronic device.

electron The basic particle of negative electrical charge.

electron-hole pair The conduction electron and the hole created when the electron leaves the valence band.

emitter The most heavily doped of the three semiconductor regions of a BJT.

emitter-follower A popular term for a common-collector amplifier.

enhancement In a MOSFET, the process of creating a channel or increasing the conductivity of the channel by the addition of charge carriers.

feedback The process of returning a portion of a circuit's output back to the input in such a way as to oppose or aid a change in the output.

feedback oscillator An electronic circuit that operates with positive feedback and produces a time-varying output signal without an external input signal.

FET Field-effect transistor; a type of unipolar, voltage-controlled transistor that uses an induced electric field to control current.

fiber optics The use of light for the transmission of information through tiny fiber cables.

filter A capacitor in a power supply used to reduce the variation of the output voltage from a rectifier; a type of circuit that passes or blocks certain frequencies to the exclusion of all others.

floating point A point in the circuit that is not electrically connected to ground or a "solid" voltage.

fold-back current limiting A method of current limiting in voltage regulators.

forced commutation A method of turning off an SCR.

forward bias The condition in which a diode conducts current.

forward-breakover voltage ($V_{BR(F)}$) The voltage at which a device enters the forward-blocking region.

4-layer diode The type of two-terminal thyristor that conducts current when the anode-to-cathode voltage reaches a specified "breakover" value.

four-quadrant multiplier A linear device that produces an output voltage proportional to the product of two input voltages.

FPAA Field-programmable analog array; an integrated circuit that can be programmed for implementation of an analog circuit design.

free electron An electron that has acquired enough energy to break away from the valence band of the parent atom; also called a conduction electron.

frequency modulation (FM) A communication method in which a lower frequency intelligence-carrying signal modulates (varies) the frequency of a higher frequency signal.

frequency response The change in gain or phase shift over a specified range of input signal frequencies.

full-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with two output pulses occurring for each input cycle.

fuse A protective device that burns open when the current exceeds a rated limit.

gain The amount by which an electrical signal is increased or amplified.

gain-bandwidth product A constant parameter which is always equal to the frequency at which the op-amp's open-loop gain is unity (1).

gate One of the three terminals of a FET analogous to the base of a BJT.

germanium A semiconductive material.

half-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with one output pulse occurring for each input cycle.

high-pass filter A type of filter that passes frequencies above a certain frequency while rejecting lower frequencies.

holding current (I_H) The value of the anode current below which a device switches from the forward-conduction region to the forward-blocking region.

hole The absence of an electron in the valence band of an atom.

host processor A microprocessor embedded in the system in which the FPAA is operating for controlling dynamic configuration.

hysteresis Characteristic of a circuit in which two different trigger levels create an offset or lag in the switching action.

IGBT Insulated-gate bipolar transistor; a device that combines features of the MOSFET and the BJT and used mainly for high-voltage switching applications.

index of refraction An optical characteristic of a material that determines the critical angle.

infrared (IR) Light that has a range of wavelengths greater than visible light.

input resistance The resistance looking in at the transistor base.

instrumentation amplifier An amplifier used for amplifying small signals riding on large common-mode voltages.

insulator A material that does not conduct current.

integrated circuit (IC) A type of circuit in which all the components are constructed on a single tiny chip of silicon.

integrator A circuit that produces an output which approximates the area under the curve of the input function.

intrinsic The pure or natural state of a material.

inverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the inverting input.

ionization The removal or addition of an electron from or to a neutral atom so that the resulting atom (called an ion) has a net positive or negative charge.

irradiance (H) The power per unit area at a specified distance for the LED; the light intensity.

isolation amplifier An amplifier with electrically isolated internal stages.

JFET Junction field-effect transistor; one of two major types of field-effect transistors.

large-signal A signal that operates an amplifier over a significant portion of its load line.

LASCR Light-activated silicon-controlled rectifier; a four-layer semiconductor device (thyristor) that conducts current in one direction when activated by a sufficient amount of light and continues to conduct until the current falls below a specified value.

laser Light amplification by stimulated emission of radiation.

light-emitting diode (LED) A type of diode that emits light when there is forward current.

limiter A diode circuit that clips off or removes part of a waveform above and/or below a specified level.

linear Characterized by a straight-line relationship.

linear region The region of operation along the load line between saturation and cutoff.

linear regulator A voltage regulator in which the control element operates in the linear region.

line regulation The change in output voltage for a given change in input (line) voltage, normally expressed as a percentage.

load The amount of current drawn from the output of a circuit through a load resistance.

load regulation The change in output voltage for a given change in load current, normally expressed as a percentage.

lock range The range of frequencies over which a PLL can maintain lock.

logarithm An exponent; the logarithm of a quantity is the exponent or power to which a given number called the base must be raised in order to equal the quantity.

look-up table (LUT) A type of memory that stores preprogrammed data for use in the configuration of an FPAA.

loop gain An op-amp's open-loop gain times the attenuation.

lower-side frequency In balanced modulation, the difference of the carrier frequency and the modulation frequency.

low-pass filter A type of filter that passes frequencies below a certain frequency while rejecting higher frequencies.

majority carrier The most numerous charge carrier in a doped semiconductive material (either free electrons or holes).

midrange gain The gain that occurs for the range of frequencies between the lower and upper critical frequencies.

minority carrier The least numerous charge carrier in a doped semiconductive material (either free electrons or holes).

mixer A device for down-converting frequencies in a receiver system.

modem A device that converts signals produced by one type of device to a form compatible with another; *modulator/demodulator*.

modulation The process in which a signal containing information is used to modify a characteristic of another signal such as amplitude, frequency, or pulse width so that the information on the first is also contained on the second.

monochromatic Related to light of a single frequency; one color.

MOSFET Metal oxide semiconductor field-effect transistor; one of two major types of FETs; sometimes called IGFET for insulated-gate FET.

multistage Characterized by having more than one stage; a cascaded arrangement of two or more amplifiers.

natural logarithm The exponent to which the base e ($e = 2.71828$) must be raised in order to equal a given quantity.

negative feedback The process of returning a portion of the output signal to the input of an amplifier such that it is out of phase with the input signal.

neutron An uncharged particle found in the nucleus of an atom.

noise An unwanted signal.

noninverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the noninverting input.

nucleus The central part of an atom containing protons and neutrons.

octave A two-times increase or decrease in the value of a quantity such as frequency.

open-loop voltage gain (A_{ol}) The voltage gain of an op-amp without external feedback.

operational amplifier (op-amp) A type of amplifier that has a very high voltage gain, very high input impedance, very low output impedance, and good rejection of common-mode signals.

operational transconductance amplifier (OTA) A voltage-to-current amplifier.

orbit The path an electron takes as it circles around the nucleus of an atom.

order The number of poles in a filter.

oscillator A circuit that produces a periodic waveform on its output with only the dc supply voltage as its input.

output resistance The resistance looking in at the transistor collector.

overall voltage gain The product of the attenuation and the gain from base to collector of an amplifier.

passband The range of frequencies that are allowed to pass through a filter with minimum attenuation.

peak inverse voltage (PIV) The maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reversed-biased.

pentavalent Describes an atom with five valence electrons.

phase-locked loop (PLL) A device for locking onto and tracking the frequency of an incoming signal.

phase margin The difference between the total phase shift through an amplifier and 180 degrees; the additional amount of phase shift that can be allowed before instability occurs.

phase shift The relative angular displacement of a time-varying function relative to a reference.

phase-shift oscillator A type of feedback oscillator that is characterized by three RC circuits in the positive feedback loop that produces a phase shift of 180° .

photodiode A diode in which the reverse current varies directly with the amount of light.

photon A particle of light energy.

phototransistor A transistor in which base current is produced when light strikes the photosensitive semiconductor base region.

piezoelectric effect The property of a crystal whereby a changing mechanical stress produces a voltage across the crystal.

pinch-off voltage The value of the drain-to-source voltage of a FET at which the drain current becomes constant when the gate-to-source voltage is zero.

p/n junction The boundary between two different types of semiconductive materials.

pole A circuit containing one resistor and one capacitor that contributes -20 dB/decade to a filter's roll-off.

positive feedback The return of a portion of the output signal to the input such that it reinforces and sustains the output. This output signal is in phase with the input signal.

power gain The ratio of output power to input power of an amplifier.

power supply A circuit that converts ac line voltage to dc voltage and supplies constant power to operate a circuit or system.

proton The basic particle of positive charge.

push-pull A type of class B amplifier with two transistors in which one transistor conducts for one half-cycle and the other conducts for the other half-cycle.

PUT Programmable unijunction transistor; a type of three-terminal thyristor (more like an SCR than a UJT) that is triggered into conduction when the voltage at the anode exceeds the voltage at the gate.

Q-point The dc operating (bias) point of an amplifier specified by voltage and current values.

quality factor (Q) For a reactive component, a figure of merit which is the ratio of energy stored and returned by the component to the energy dissipated; for a band-pass filter, the ratio of the center frequency to its bandwidth.

radiant intensity (I_e) The output power of an LED per steradian in units of mW/sr.

radiation The process of emitting electromagnetic or light energy.

recombination The process of a free (conduction band) electron falling into a hole in the valence band of an atom.

rectifier An electronic circuit that converts ac into pulsating dc; one part of a power supply.

regulator An electronic device or circuit that maintains an essentially constant output voltage for a range of input voltage or load values; one part of a power supply.

relaxation oscillator An electronic circuit that uses an RC timing circuit to generate a nonsinusoidal waveform without an external input signal.

reverse bias The condition in which a diode prevents current.

ripple factor A measure of effectiveness of a power supply filter in reducing the ripple voltage; ratio of the ripple voltage to the dc output voltage.

ripple voltage The small variation in the dc output voltage of a filtered rectifier caused by the charging and discharging of the filter capacitor.

r parameter One of a set of BJT characteristic parameters that include α_{DC} , β_{DC} , r'_e , r'_b , and r'_c .

roll-off The rate of decrease in the gain above or below the critical frequencies of a filter.

saturation The state of a BJT in which the collector current has reached a maximum and is independent of the base current.

schematic A symbolized diagram representing an electrical or electronic circuit.

Schmitt trigger A comparator with hysteresis.

SCR Silicon-controlled rectifier; a type of three-terminal thyristor that conducts current when triggered on by a voltage at the single gate terminal and remains on until the anode current falls below a specified value.

SCS Silicon-controlled switch; a type of four-terminal thyristor that has two gate terminals that are used to trigger the device on and off.

semiconductor A material that lies between conductors and insulators in its conductive properties.

shadow RAM A random-access memory used in FPAs for temporarily holding data while the device is operating and before it is loaded into the configuration RAM for reprogramming.

shell An energy band in which electrons orbit the nucleus of an atom.

signal compression The process of scaling down the amplitude of a signal voltage.

silicon A semiconductive material.

single-ended mode A mode of op-amp operation in which a signal voltage is applied to only one input.

slew rate The rate of change of the output voltage of an op-amp in response to a step input.

source One of the three terminals of a FET analogous to the emitter of a BJT.

source-follower The common-drain amplifier.

spectral Pertaining to a range of frequencies.

stability A measure of how well an amplifier maintains its design values (Q-point, gain, etc.) over changes in beta and temperature.

stage One of the amplifier circuits in a multistage configuration.

standoff ratio The characteristic of a UJT that determines its turn-on point.

summing amplifier An op-amp configuration with two or more inputs that produces an output voltage that is proportional to the negative of the algebraic sum of its input voltages.

suppressed-carrier modulation A form of amplitude modulation in which the carrier is suppressed; also called *balanced modulation*.

switched-capacitor circuit A combination of a capacitor and transistor switches used in programmable analog devices to emulate resistors.

switching current (I_s) The value of anode current at the point where the device switches from the forward-blocking region to the forward-conduction region.

switching regulator A voltage regulator in which the control element operates as a switch.

thermal overload A condition in a rectifier where the internal power dissipation of the circuit exceeds a certain maximum due to excessive current.

thermistor A temperature-sensitive resistor with a negative temperature coefficient.

thyristor A class of four-layer (*pnpn*) semiconductor devices.

transconductance (g_m) The ratio of a change in drain current to a change in gate-to-source voltage in a FET; in general, the ratio of the output current to the input voltage.

transistor A semiconductive device used for amplification and switching applications.

triac A three-terminal thyristor that can conduct current in either direction when properly activated.

trigger The activating input of some electronic devices and circuits.

trivalent Describes an atom with three valence electrons.

troubleshooting A systematic process of isolating, identifying, and correcting a fault in a circuit or system.

tuning ratio The ratio of varactor capacitances at minimum and at maximum reverse voltages.

UJT Unijunction transistor: a three-terminal single *pn* junction device that exhibits a negative resistance characteristic.

upper-side frequency In balanced modulation, the sum of the carrier frequency and the modulated frequency.

valence Related to the outer shell of an atom.

varactor A variable capacitance diode.

V-I characteristic A curve showing the relationship of diode voltage and current.

voltage-controlled oscillator (VCO) A type of relaxation oscillator whose frequency can be varied by a dc control voltage; an oscillator for which the output frequency is dependent on a controlling input voltage.

voltage-follower A closed-loop, noninverting op-amp with a voltage gain of 1.

voltage multiplier A circuit using diodes and capacitors that increases the input voltage by two, three, or four times.

wavelength The distance in space occupied by one cycle of an electromagnetic or light wave.

Wien bridge oscillator A type of feedback oscillator that is characterized by an *RC* lead-lag circuit in the positive feedback loop.

zener breakdown The lower voltage breakdown in a zener diode.

zener diode A diode designed for limiting the voltage across its terminals in reverse bias.

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